

Compal Confidential

STORM M/B Schematic

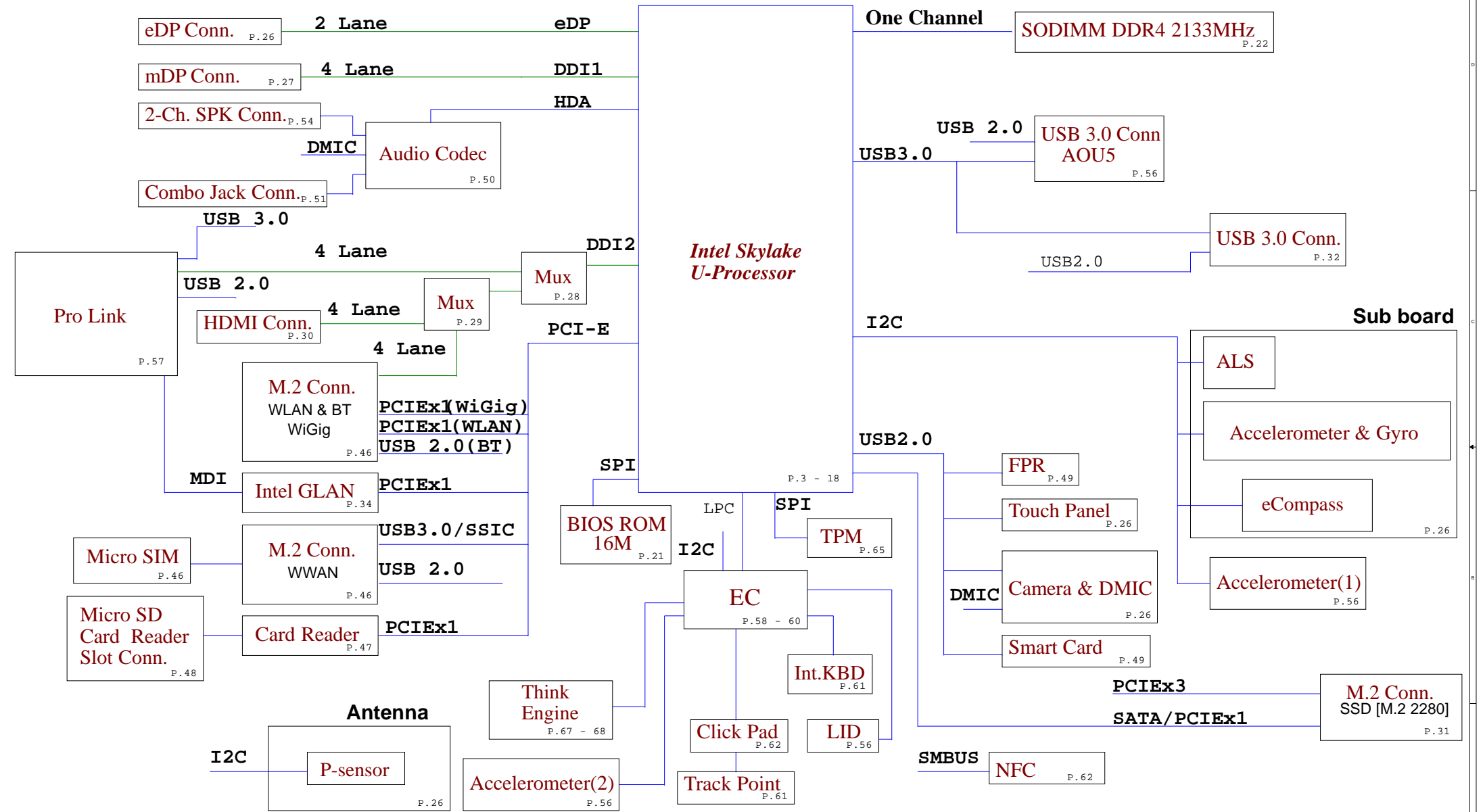
LA-C581P

Rev: 1.0_D

2015.08.13

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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	COVER PAGE
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STORM Block-Diagram



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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	BLOCK DIAGRAM
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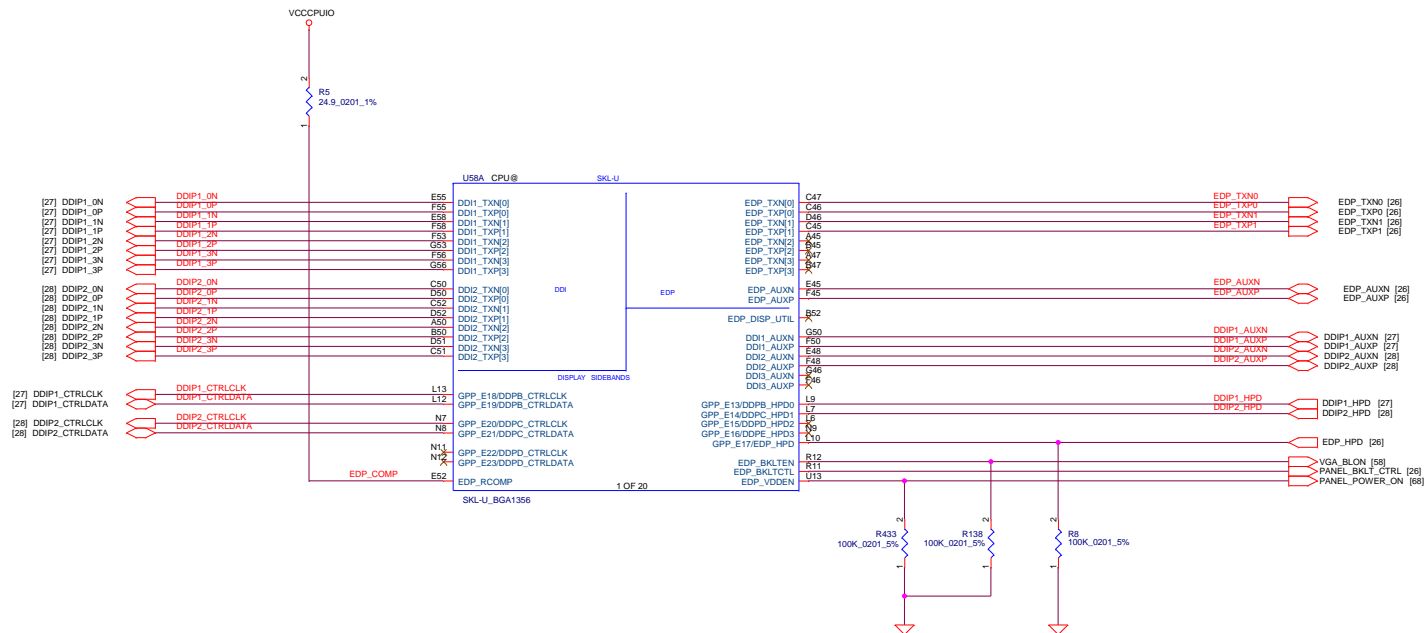
TABLE : Function Strap

DDPB_CTRLDATA

HIGH Port B is detected.
LOW Port B is not detected.

DDPC_CTRLDATA

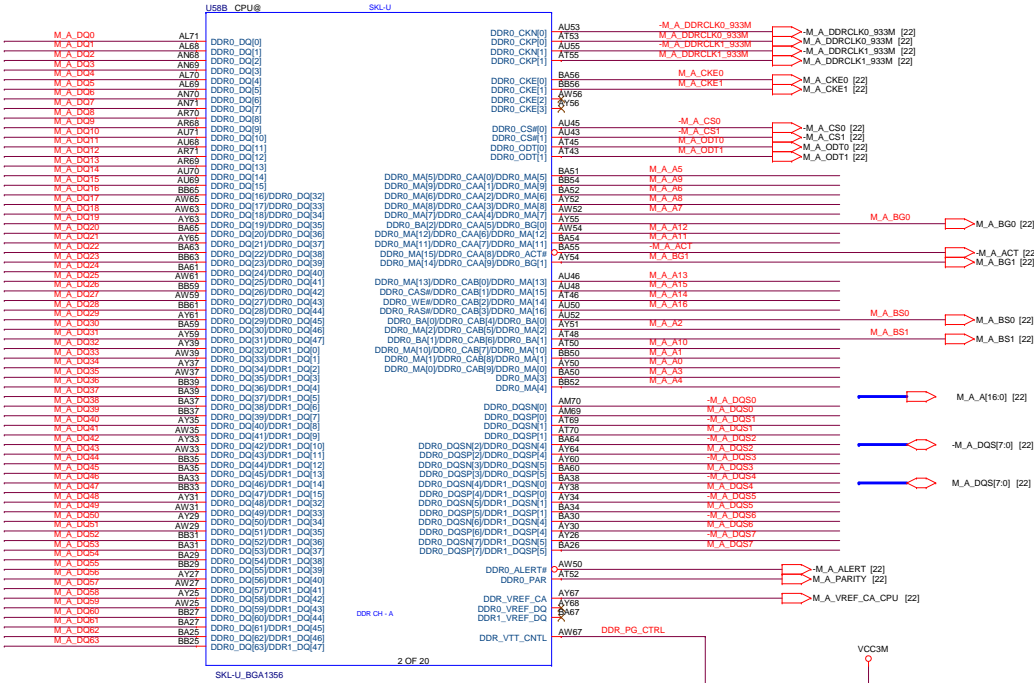
HIGH Port C is detected.
LOW Port C is not detected.



TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

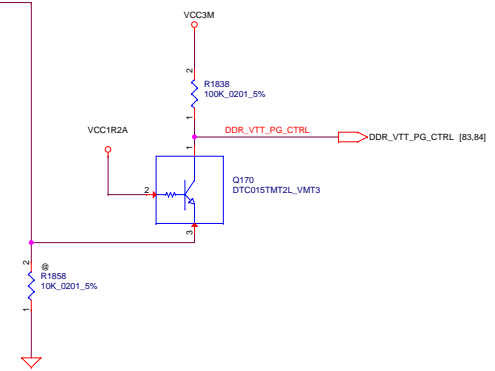
LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSN[0]	DDR0_DQSN[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSN[3]	DDR0_DQSN[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSN[5]	DDR1_DQSN[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSN[7]	DDR1_DQSN[5]

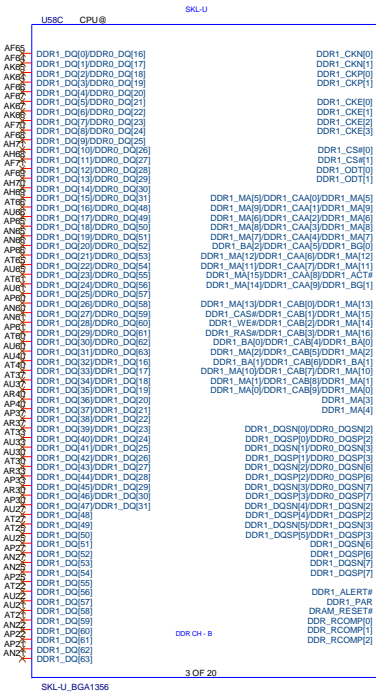
LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP64	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AT37	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT[11]
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CASH	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WER	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

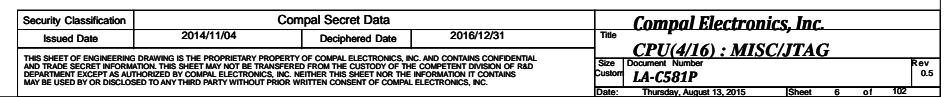


TABLE : Funct i ond Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Funct i ond Strap

SPI0_MISO (JTAG ODT Diabie)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Funct i onal Str ap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Funct i onal Str ap

GPP_C2/SMBALERT# (TLS Conf i dent i d i t y)	
HIGH	Enable ME Crypto TLS with Conf i dent i d i t y
LOW	Disable ME Crypto TLS (Default)

← LOGIC

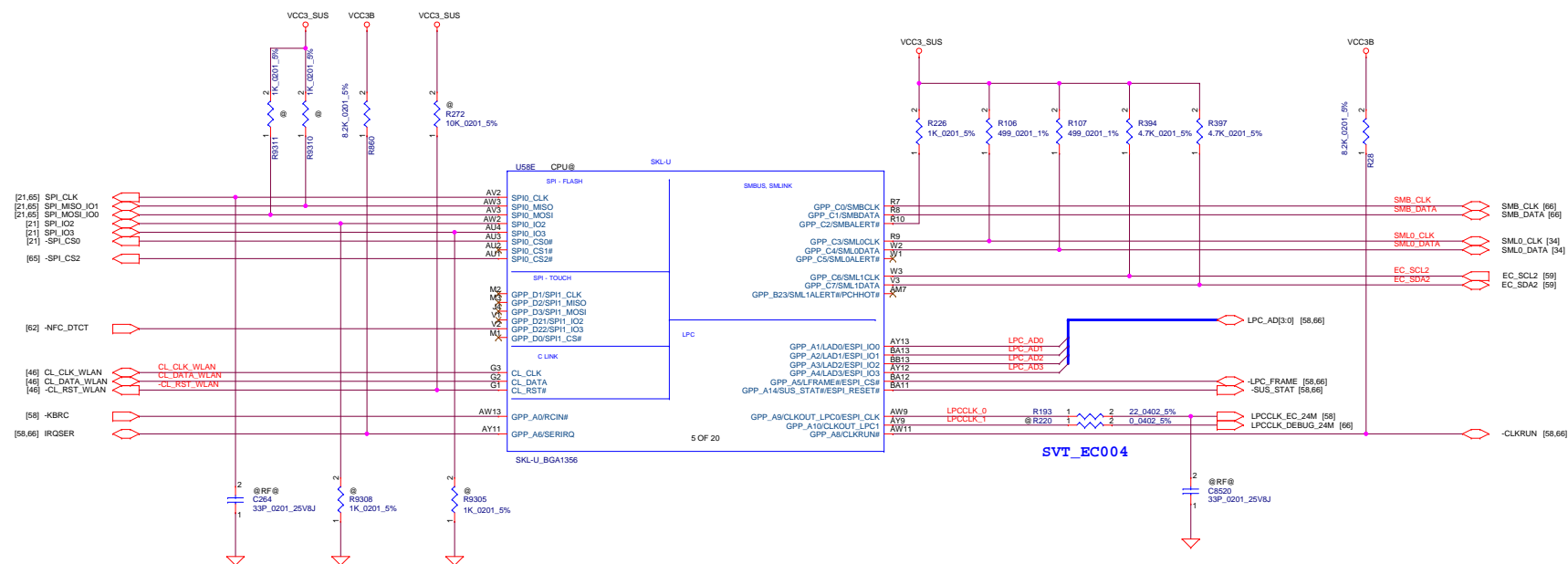


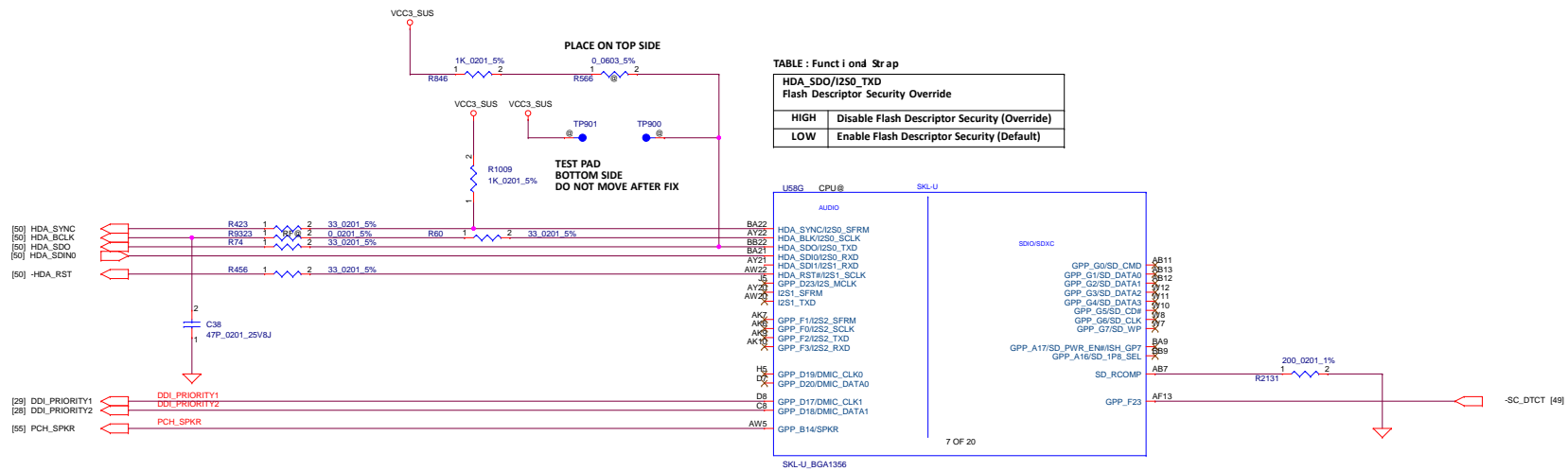
TABLE : Funct i onal Str ap

SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Funct i onal Str ap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

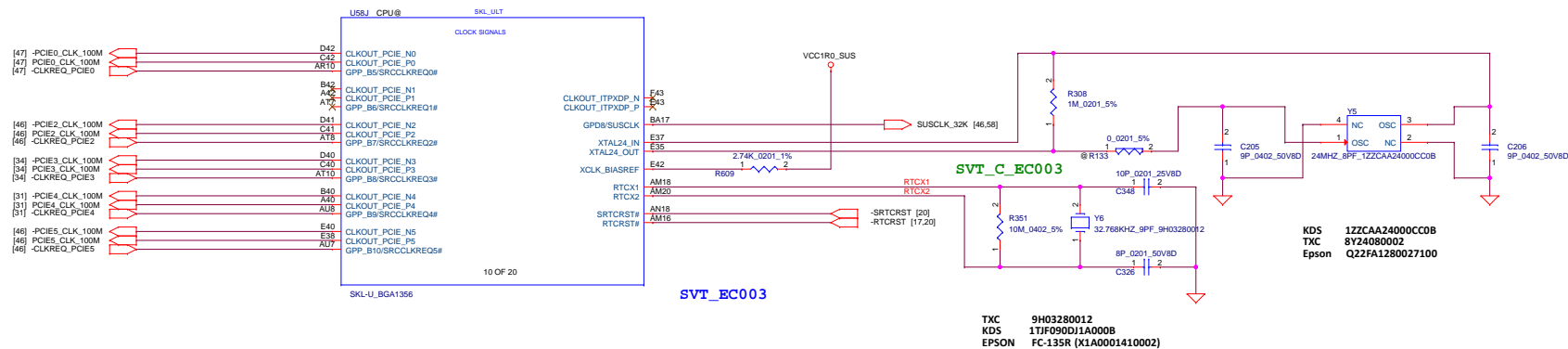
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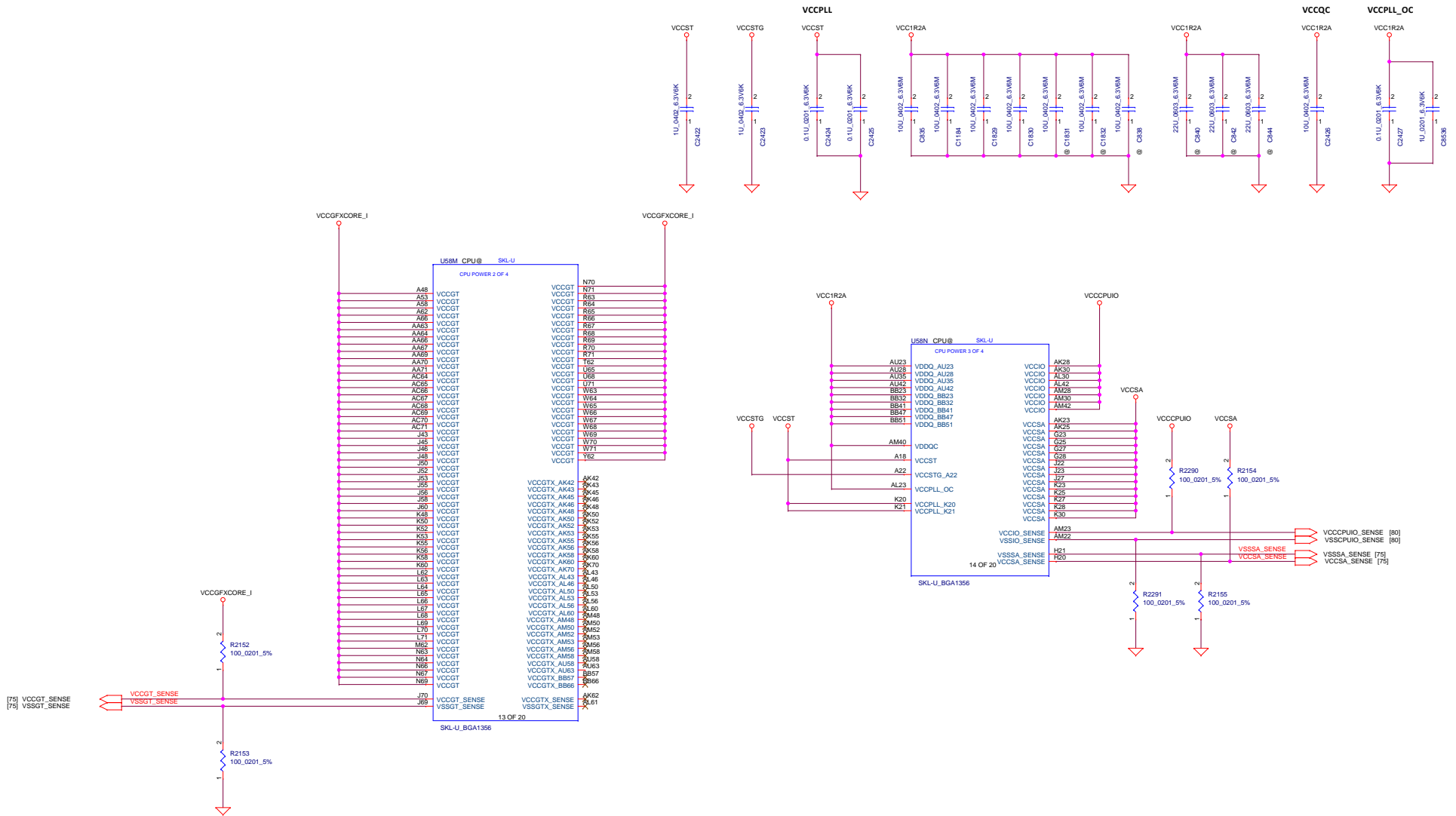
HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

LOGIC

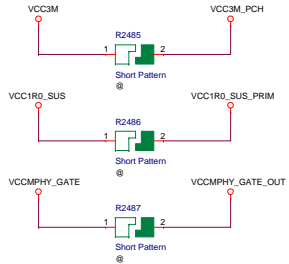


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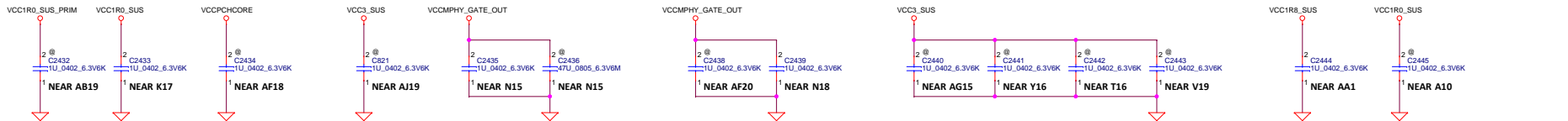
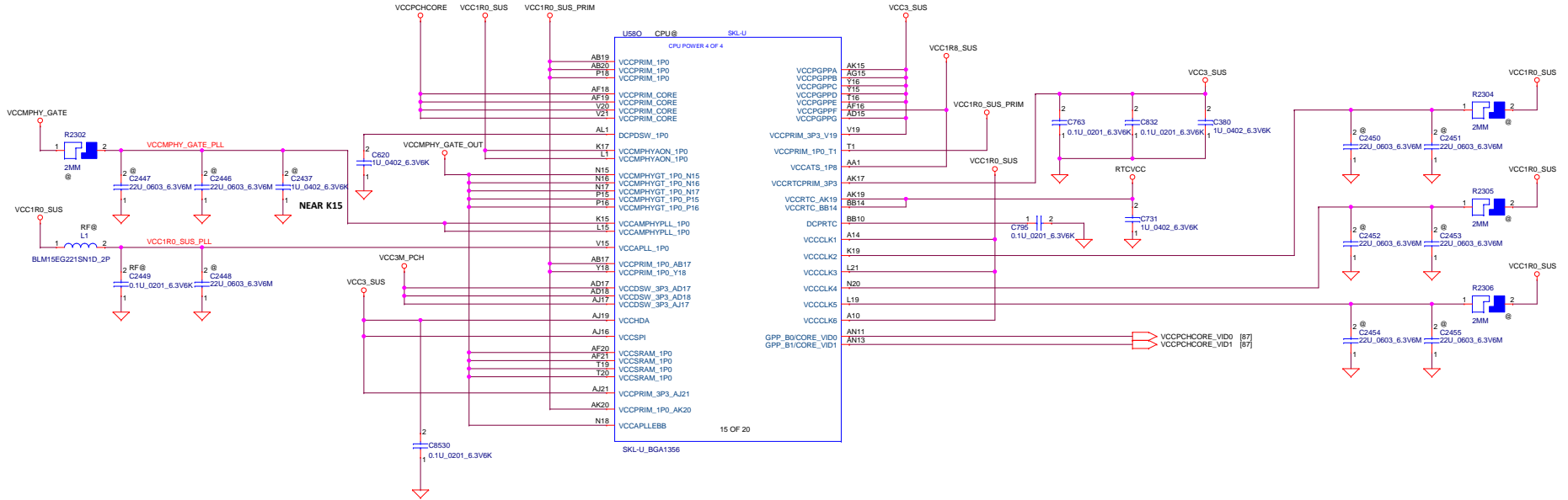
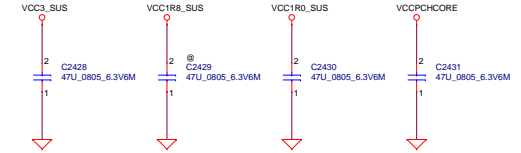
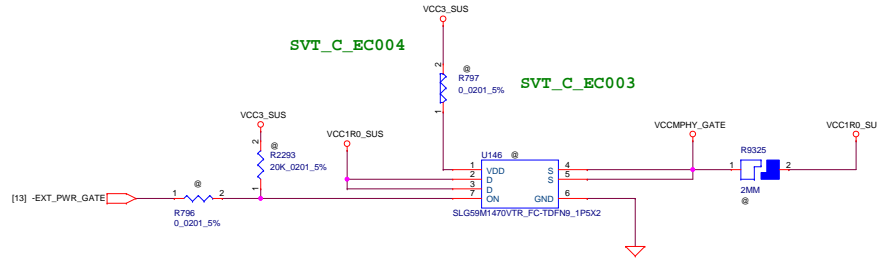
SVT_C_EC005

Short Pattern: R2485, R2486, R2487

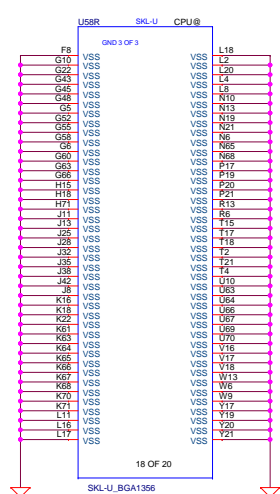
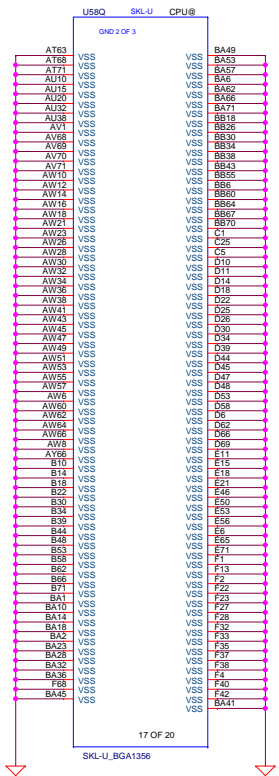
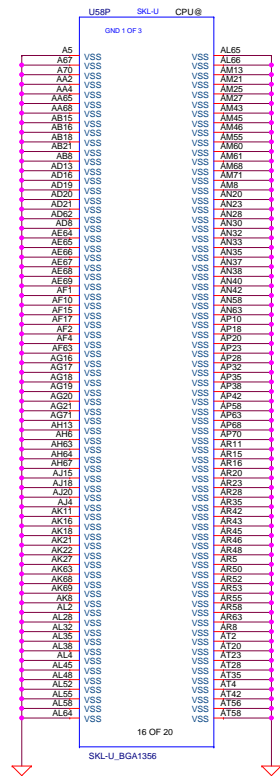


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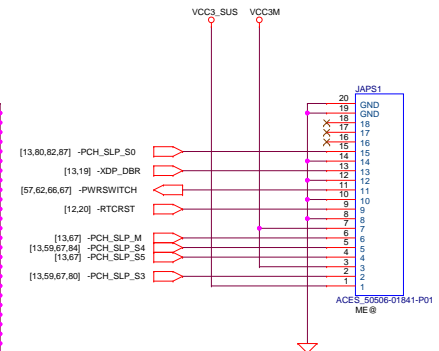
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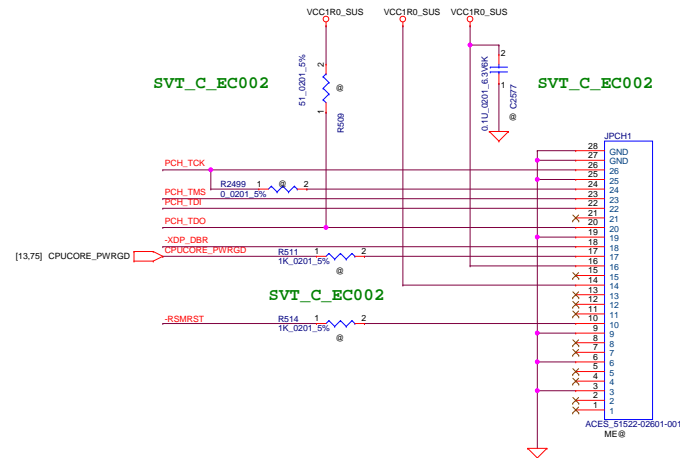
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	CPU : PCH POWER
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APS/PETS Interface

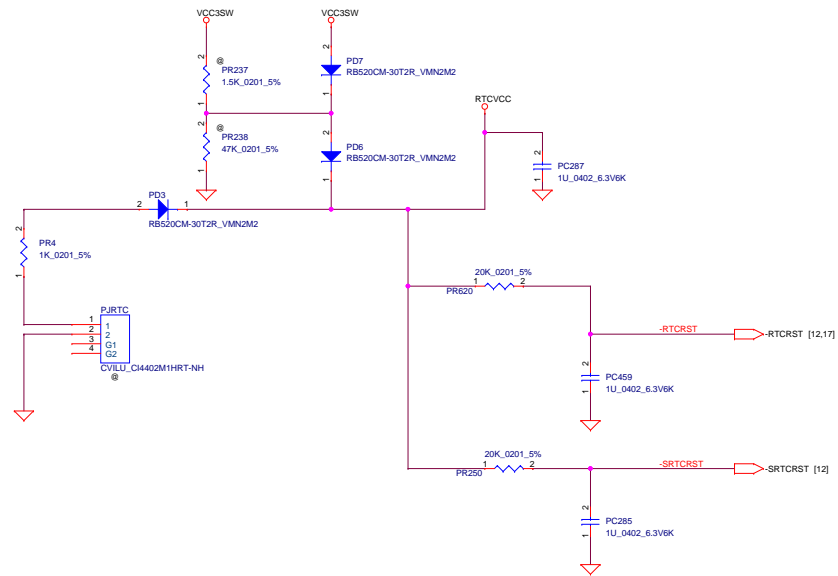


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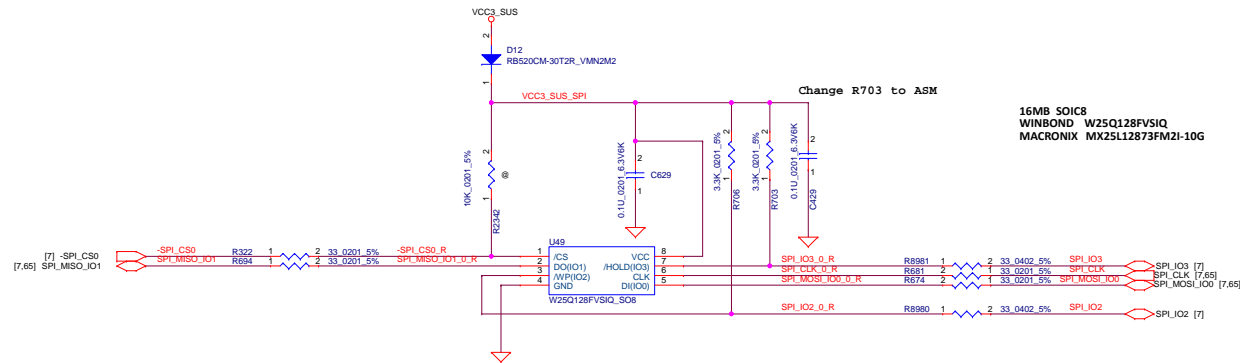


	Individual Port	Merged Port	DCI 2.0 w/o Connect
R2	ASM	ASM	ASM
R471	ASM	NO_ASM	NO_ASM
R541	ASM	NO_ASM	NO_ASM
R515	ASM	NO_ASM	NO_ASM
R530	ASM	NO_ASM	NO_ASM
R475	ASM	ASM	ASM
J8	ASM	ASM	NO_ASM
C8320	ASM	ASM	NO_ASM
R491	ASM	ASM	ASM
R588	ASM	ASM	NO_ASM
R594	ASM	ASM	NO_ASM
R2499	NO_ASM	NO_ASM	NO_ASM
R509	ASM	NO_ASM	NO_ASM
J9	ASM	ASM	NO_ASM
C2577	ASM	ASM	NO_ASM
R511	ASM	ASM	NO_ASM
R514	ASM	ASM	NO_ASM
R2493	NO_ASM	ASM	ASM
R2494	NO_ASM	ASM	NO_ASM
R2495	NO_ASM	ASM	ASM
R2496	NO_ASM	ASM	ASM
R2497	NO_ASM	ASM	ASM
R2498	NO_ASM	ASM	ASM

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				Date: Thursday, August 13, 2015	Sheet 19 of 102



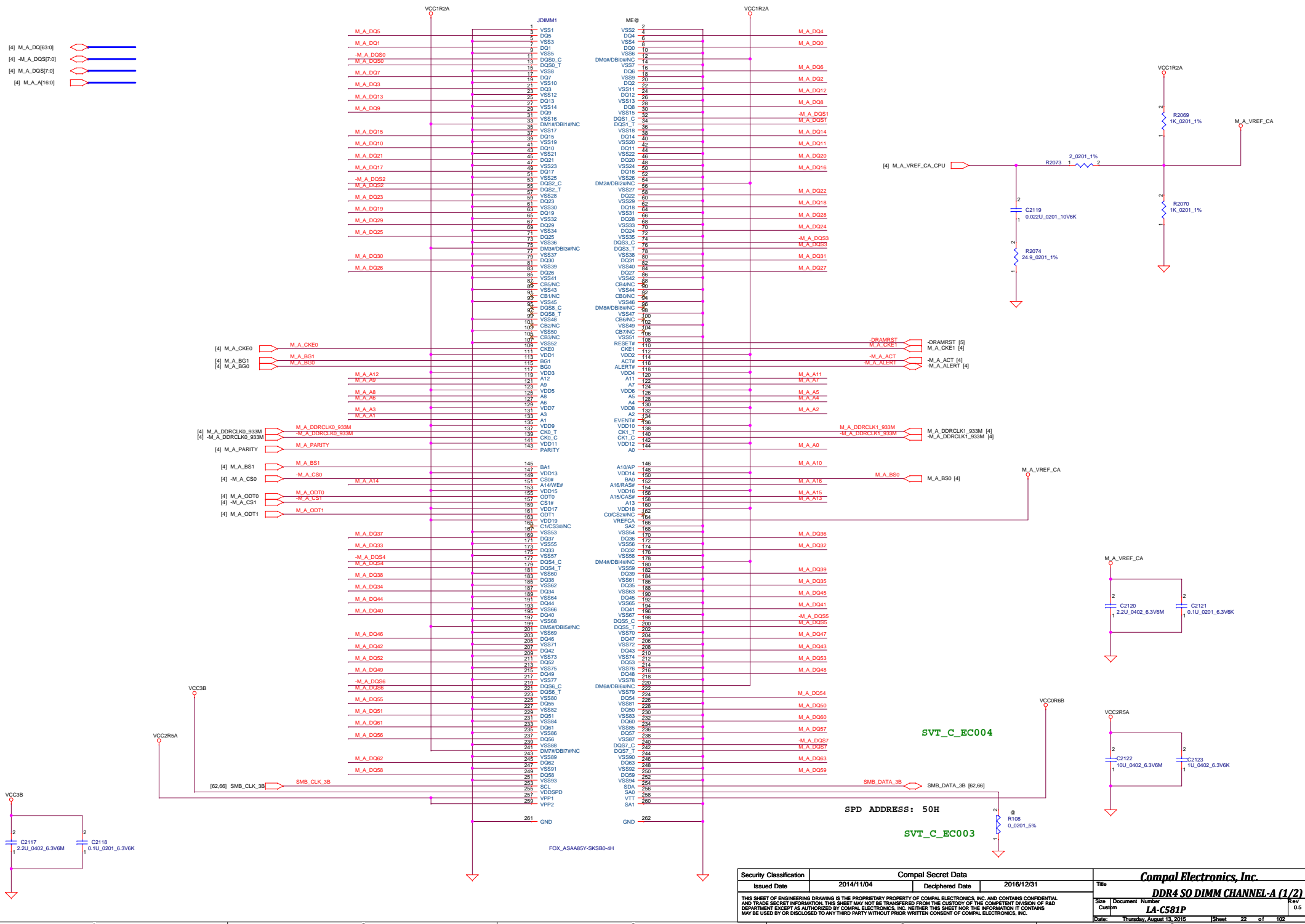
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Issued Date		2014/11/04	Deciphered Date	2016/12/31	Title
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		Custom		LA-C581P	0.1
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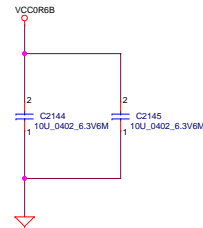
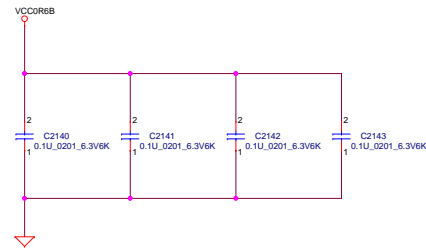
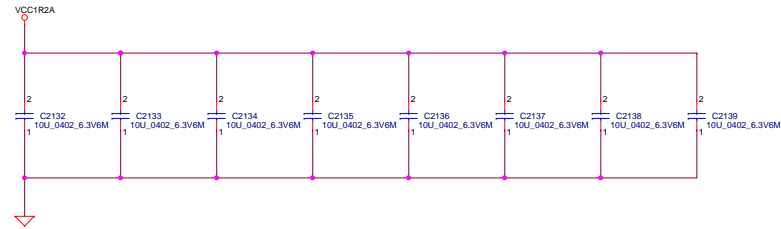
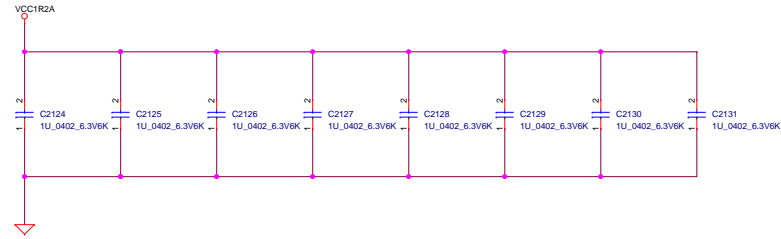
TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

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Size	Custom	Document Number	LA-C581P	Date	Thursday, August 13, 2015
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				Custom	LA-C581P	
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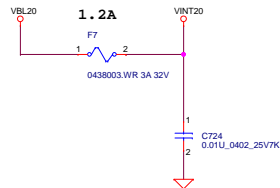
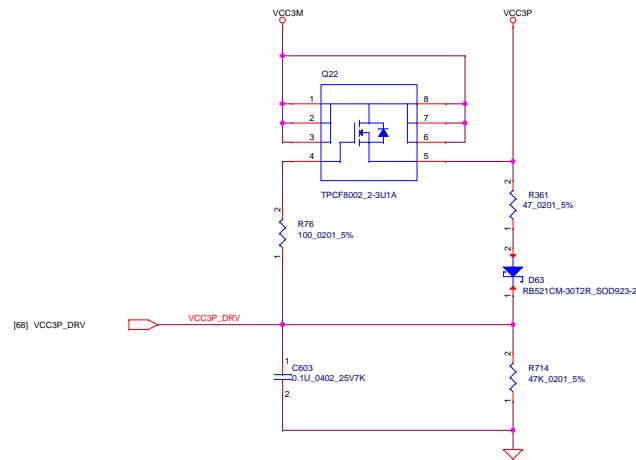
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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				Document Number	0.5
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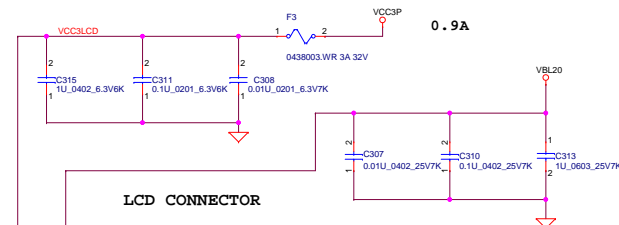
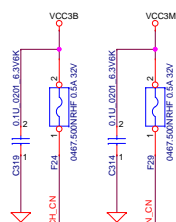
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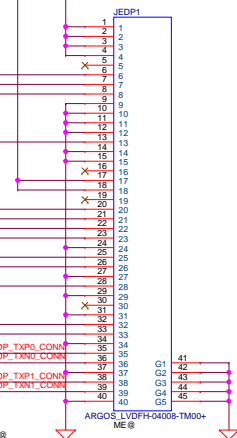
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SVT_C_EC029



LCD CONNECTOR

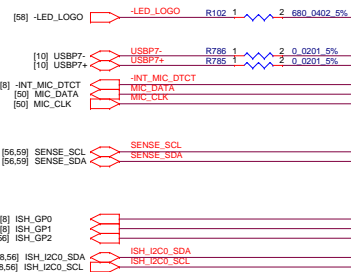


LOGO LED

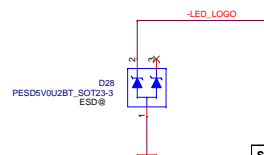
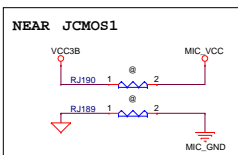
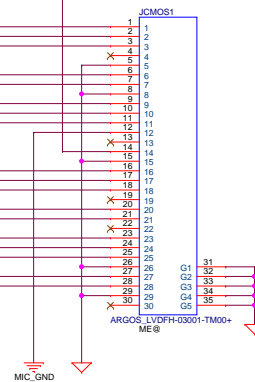
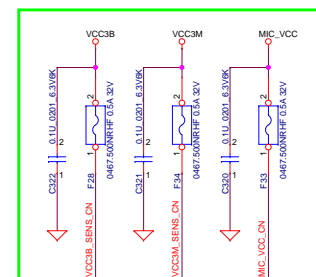
CAMERA BOARD

P-SENSOR

SENSOR BOARD



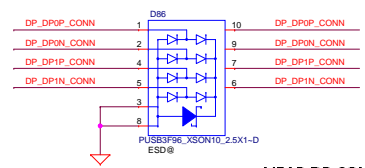
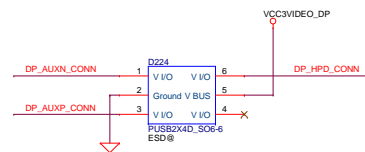
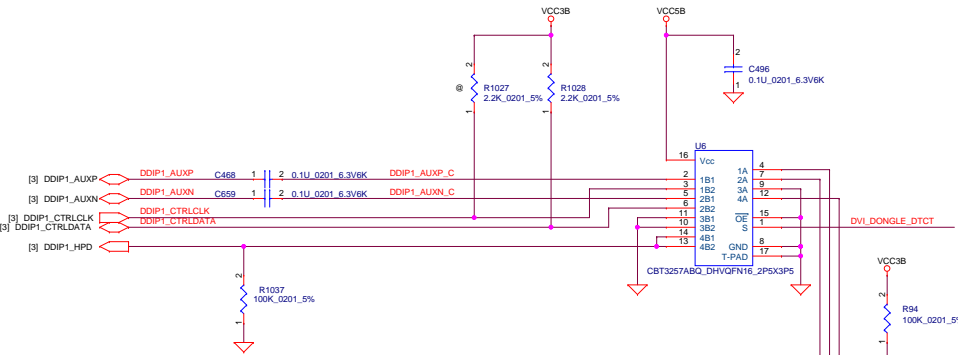
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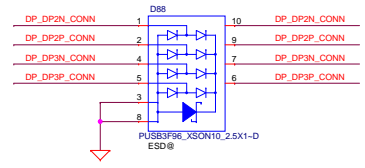
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				Documen	LA-C581P
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FOR SYSTEM DP NEAR DP CONN

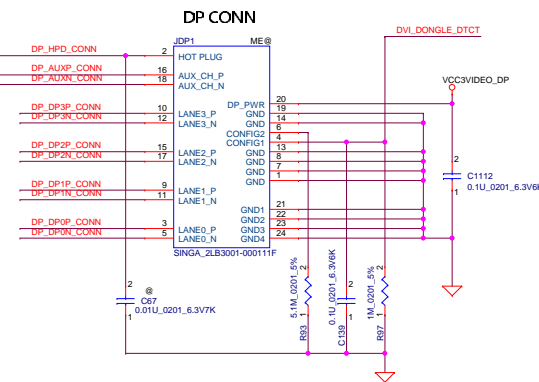
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[3] DDIP1_3P	C339	1	2	0.1U_0201_6.3V6K	DP_DP3P_CONN
[3] DDIP1_2N	C312	1	2	0.1U_0201_6.3V6K	DP_DP2N_CONN
[3] DDIP1_2P	C312	1	2	0.1U_0201_6.3V6K	DP_DP2P_CONN
[3] DDIP1_1N	C277	1	2	0.1U_0201_6.3V6K	DP_DP1N_CONN
[3] DDIP1_1P	C276	1	2	0.1U_0201_6.3V6K	DP_DP1P_CONN
[3] DDIP1_0N	C218	1	2	0.1U_0201_6.3V6K	DP_DP0N_CONN
[3] DDIP1_0P	C226	1	2	0.1U_0201_6.3V6K	DP_DP0P_CONN



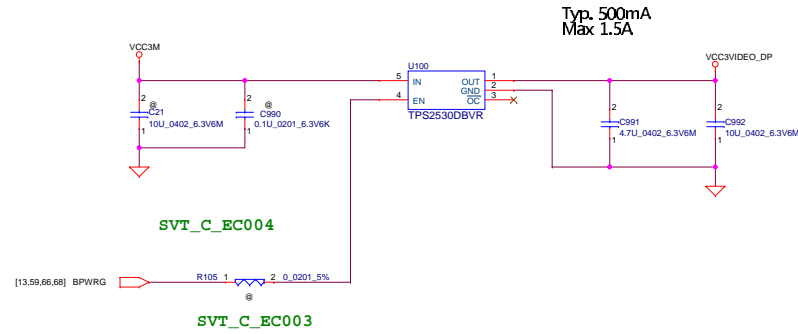
NEAR DP CONN



NEAR DP CONN



NEAR DP CONN



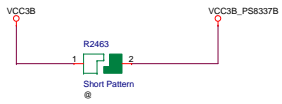
SVT_C_EC004

SVT_C_EC003

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SVT_C_EC005
Short Pattern: R2463



Place 0.1uF caps near each VDD33 pin of PS8337

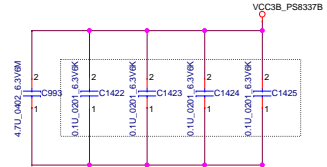
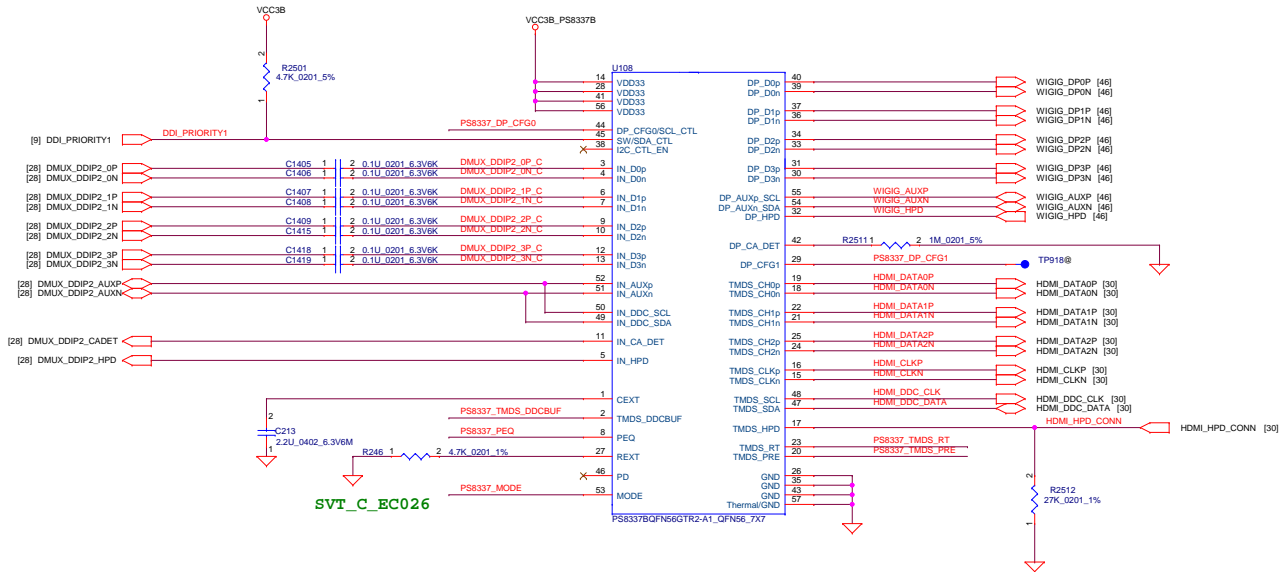


TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged
H TMDs Port has higher priority when both ports are plugged



TMDs DDCBUF (INT PD)	R1876	R1898
DDC Active Buffer	ASM	NO_ASM
DDC Pass Through w/ PU	ASM	ASM
DDC Pass Through w/o PU	NO_ASM	NO_ASM

LOGIC

PEQ (INT PD)	R1875	R1897
HEQ 15dB	ASM	NO_ASM
LLEQ 5dB	ASM	ASM
LEQ 12dB	NO_ASM	NO_ASM

LOGIC

TMDs PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

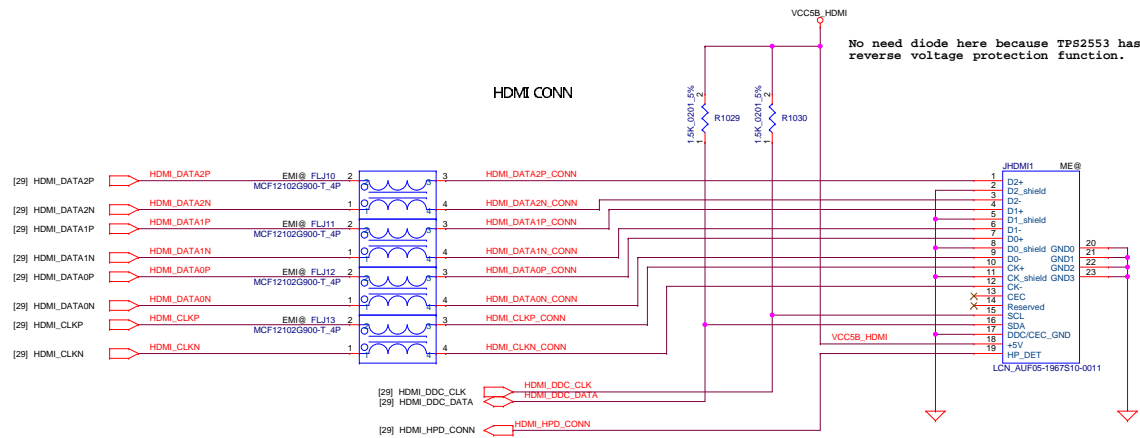
LOGIC

MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

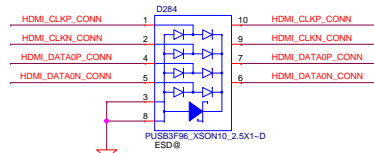
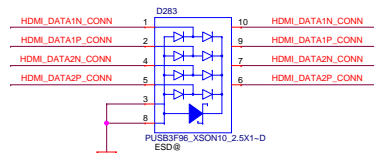
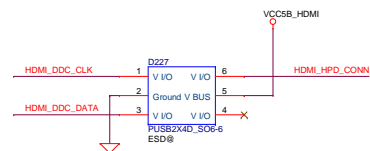
LOGIC

TMDs RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

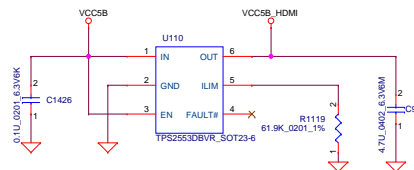
LOGIC



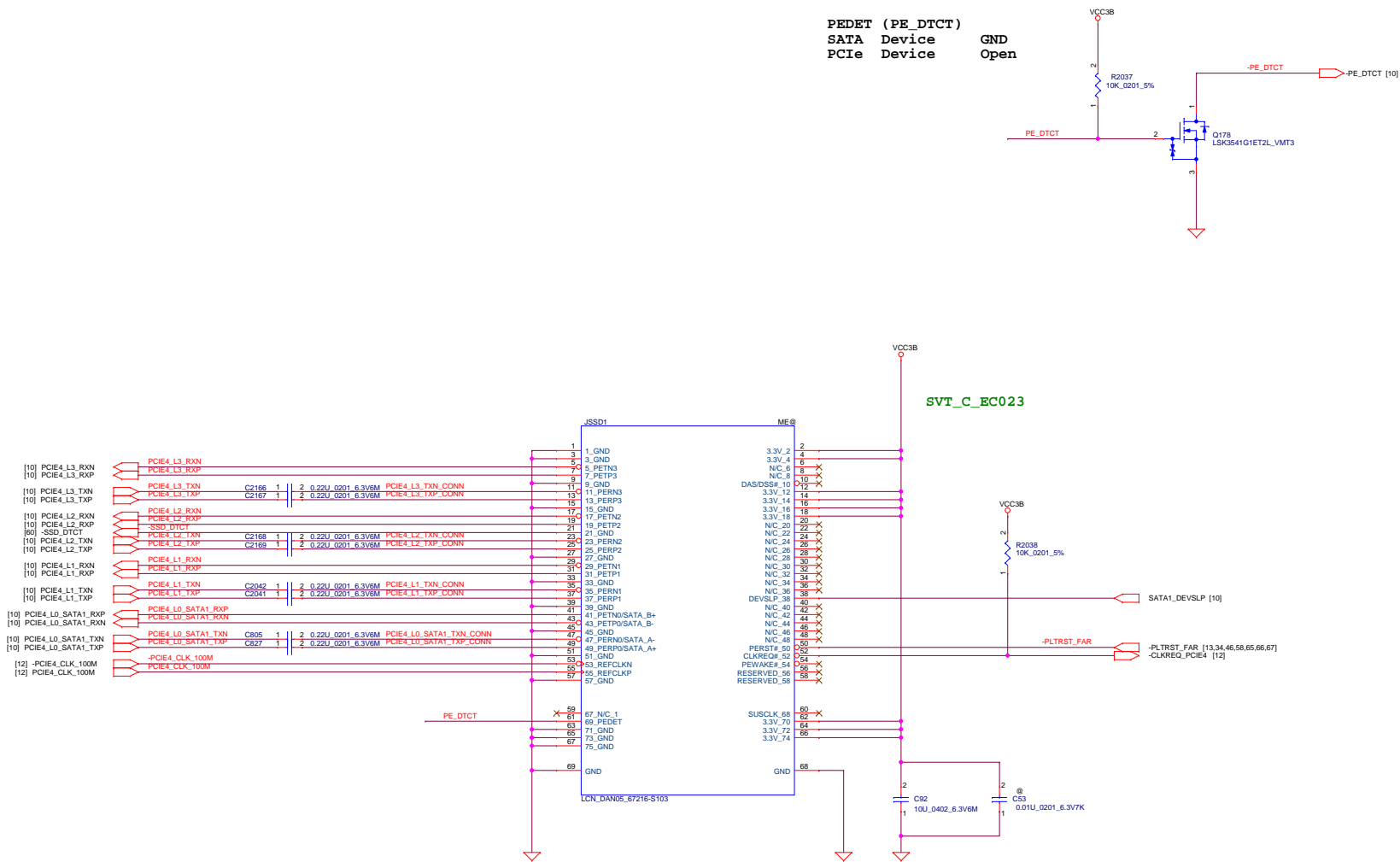
No need diode here because TPS2553 has reverse voltage protection function.



Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA



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				Customer	LA-C581P
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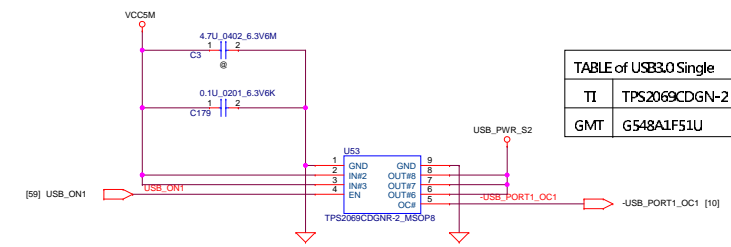
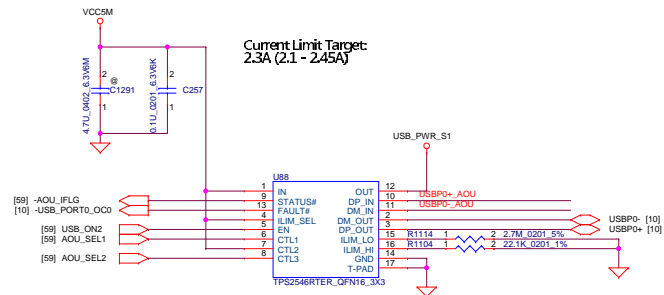
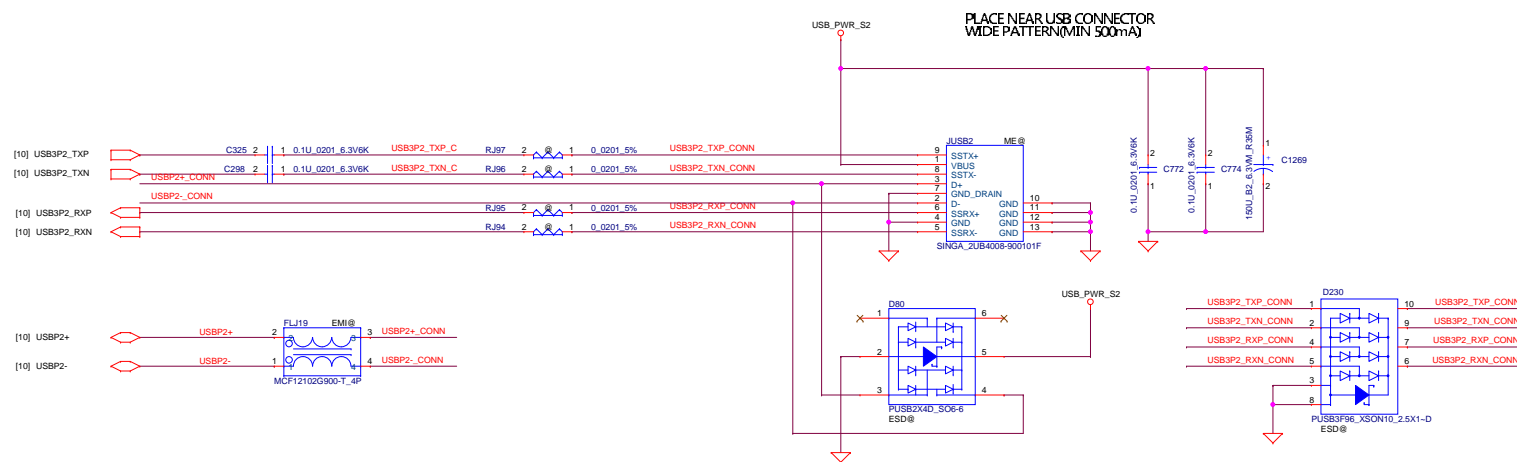
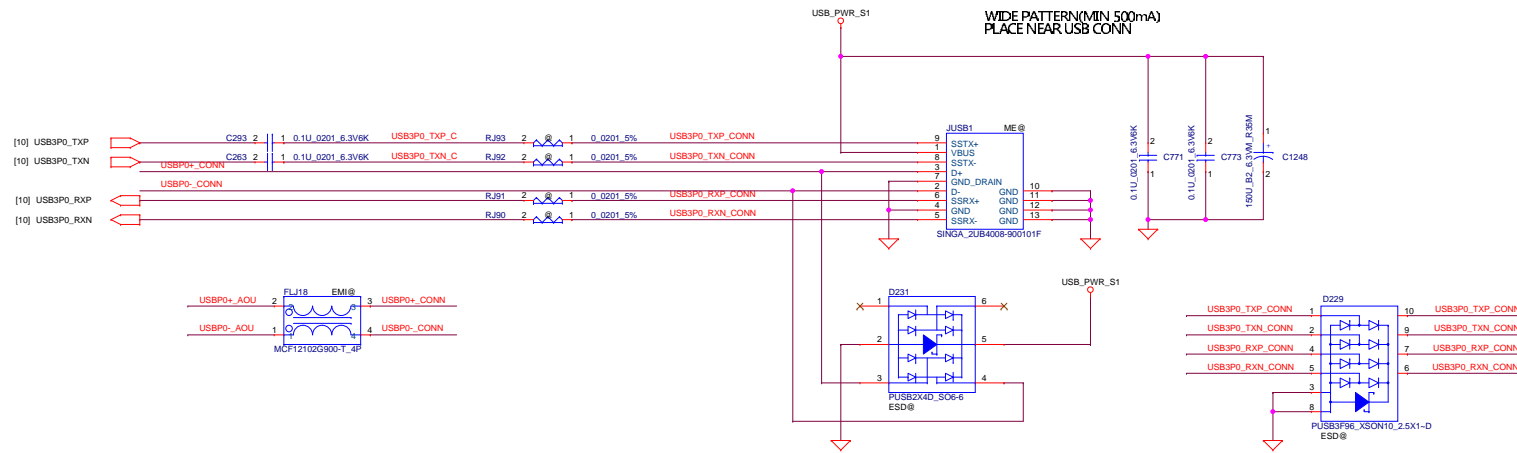


TABLE of USB3.0 Single	
TI	TPS2069CDGN-2
GMT	G548A1F51U

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				Date: Thursday, August 13, 2015	Sheet 41 of 102

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				Date: Thursday, August 13, 2015	Sheet 42 of 102

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				Custom LA-C581P	0.5
				Date: Thursday, August 13, 2015	Sheet 43 of 102

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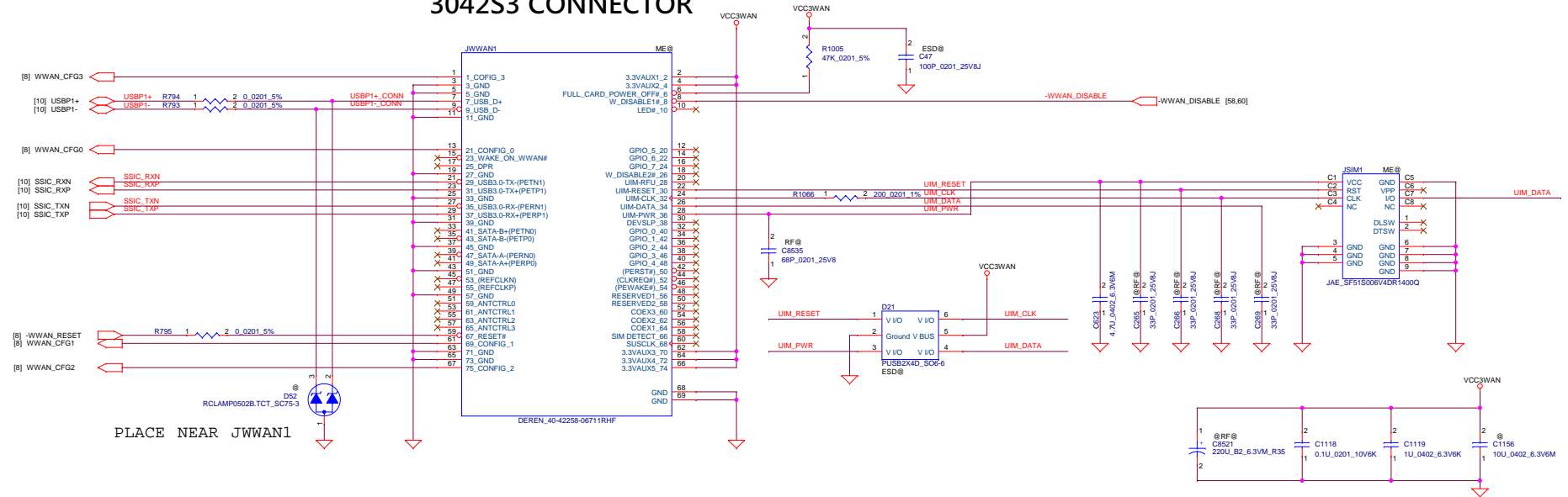
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				Date: Thursday, August 13, 2015	Sheet 45 of 102

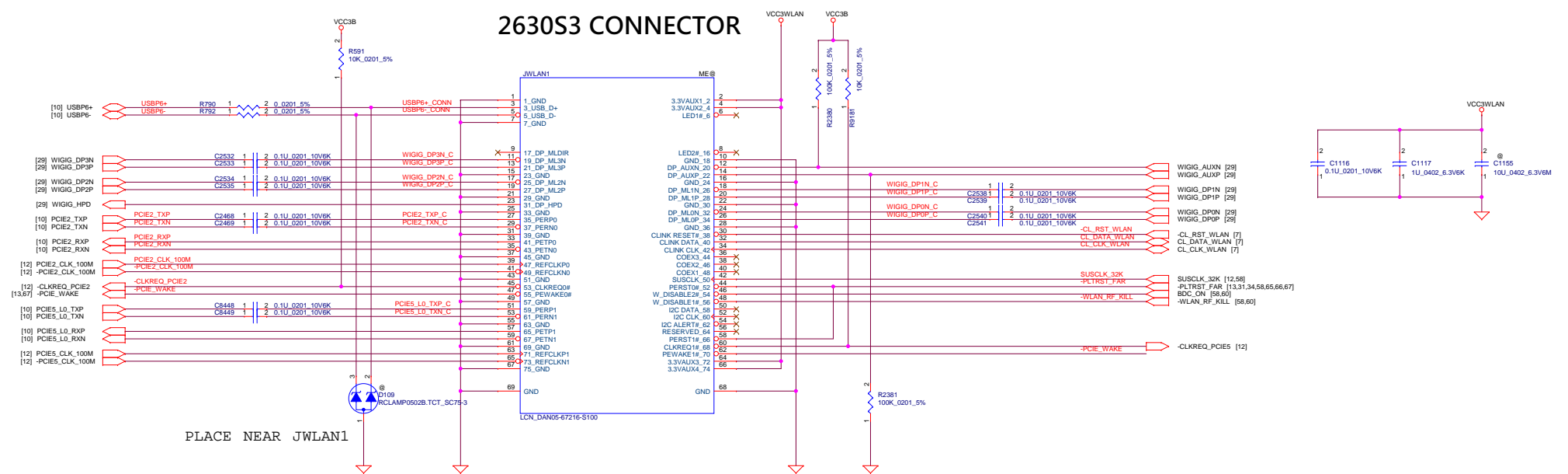
TYPE-B M.2 CARD FOR WWAN

3042S3 CONNECTOR



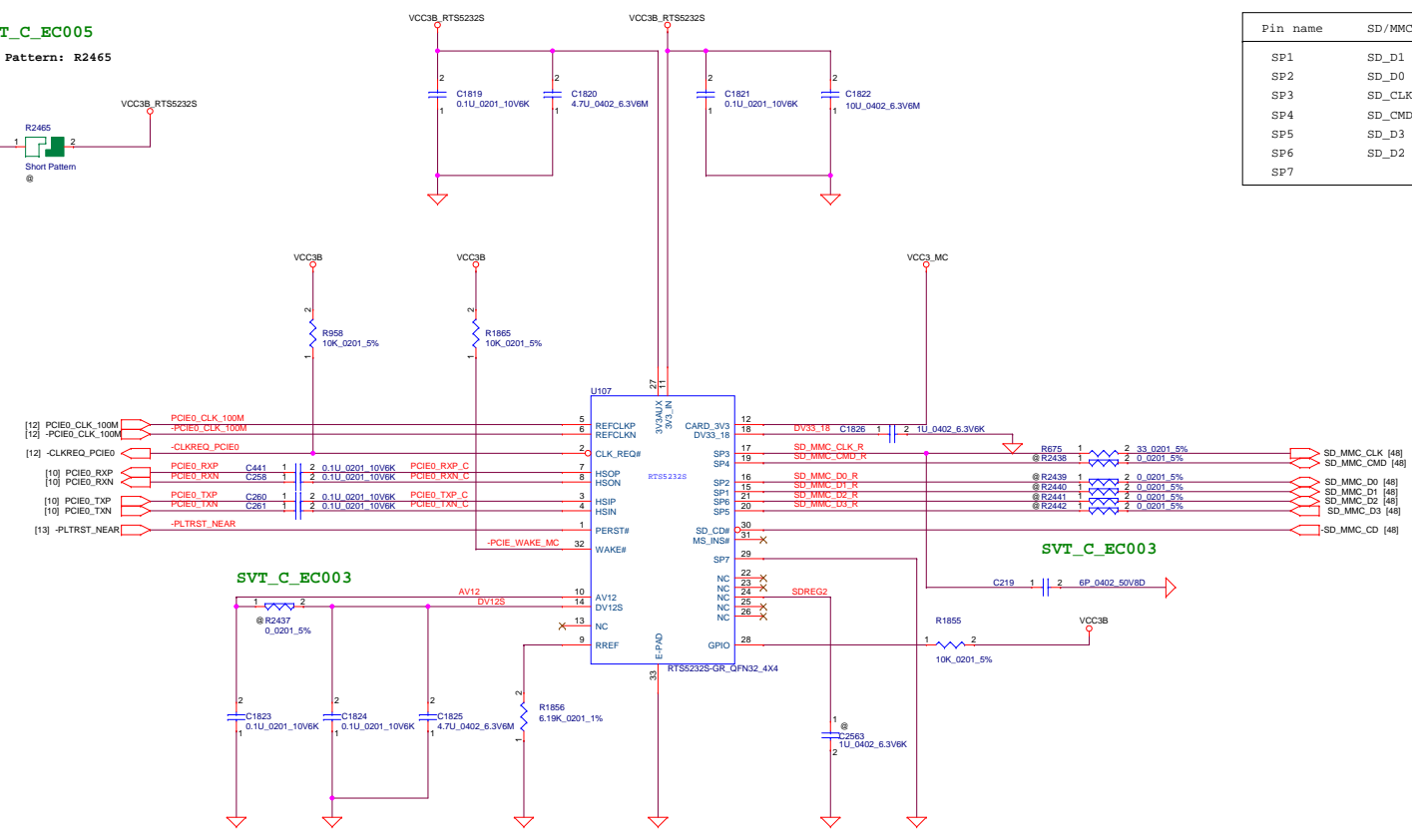
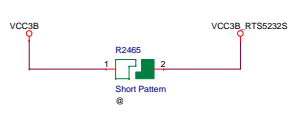
TYPE-A M.2 CARD FOR WLAN / Bluetooth / WiGig

2630S3 CONNECTOR



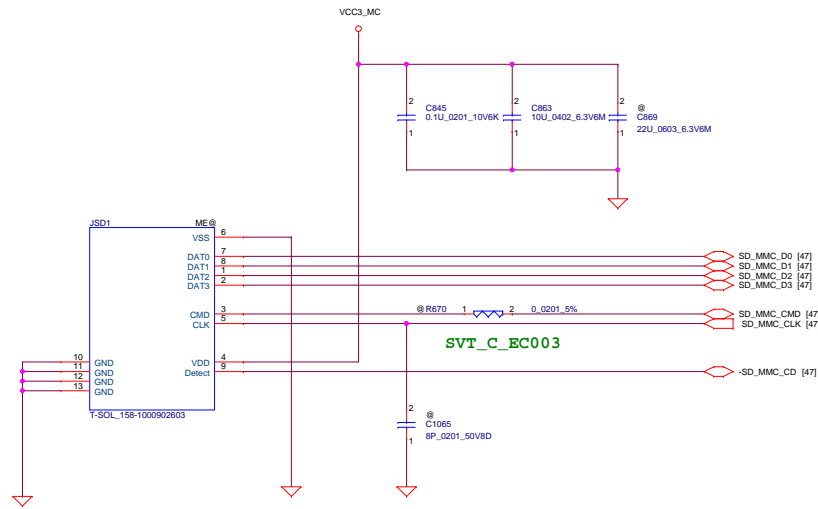
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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Customer		LA-C581P		0.5	
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SVT_C_EC005
Short Pattern: R2465

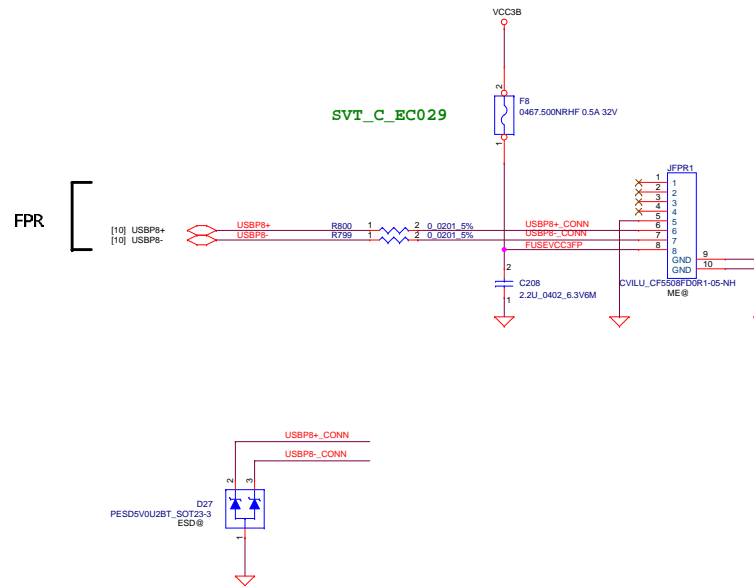
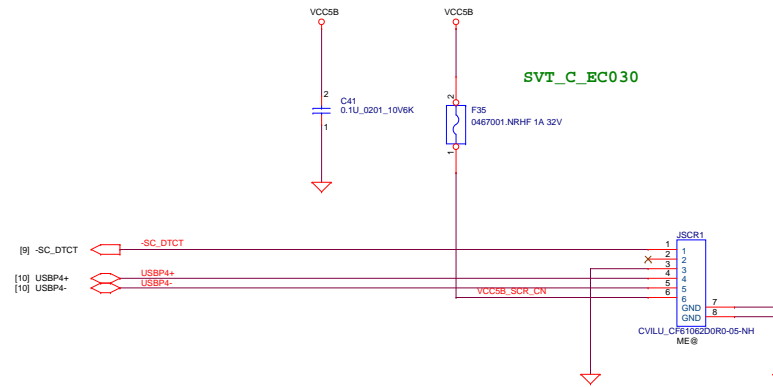


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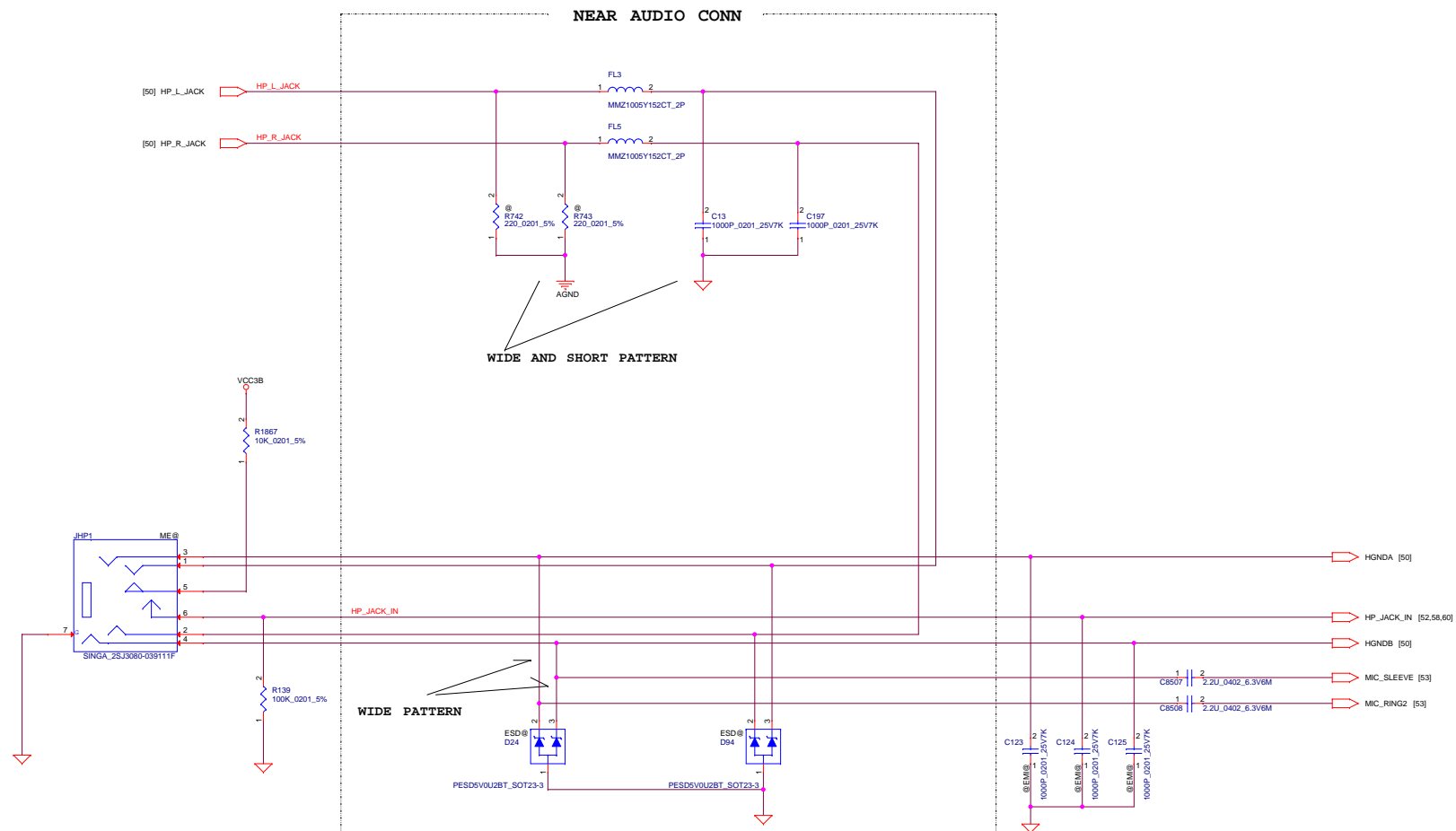
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SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		



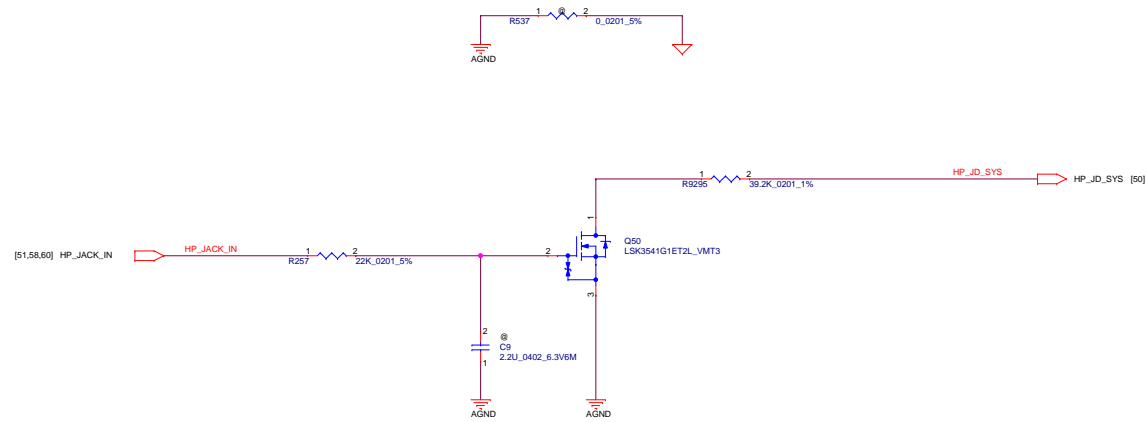
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Issued Date		2014/11/04		Title	
		Deciphered Date		2016/12/31	
				MEDIA CARD INTERFACE	
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		Docu		0.5	
		Number		LA-C581P	
		Date		Thursday, August 13, 2015	
		Sheet		48 of 102	



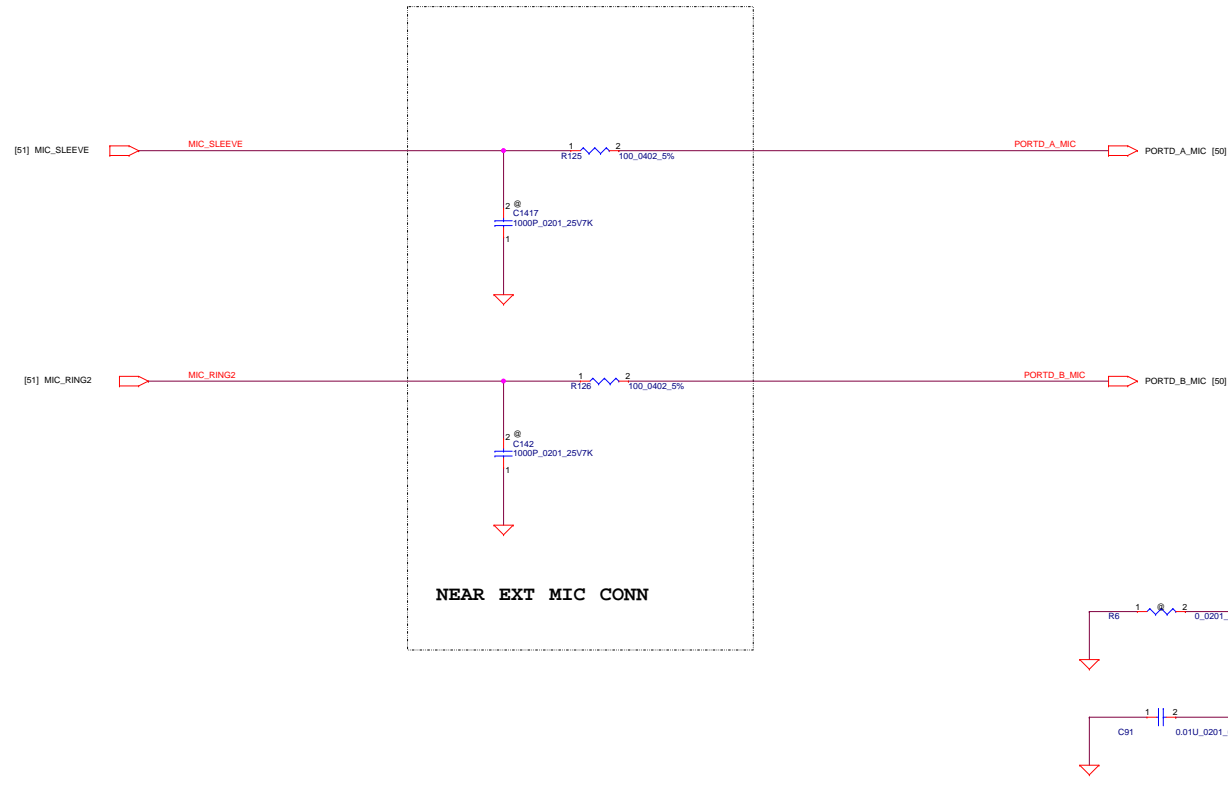
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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				Document Number	0.5
				Custom	LA-C581P
				Date	Thursday, August 13, 2015
				Sheet	49 of 102



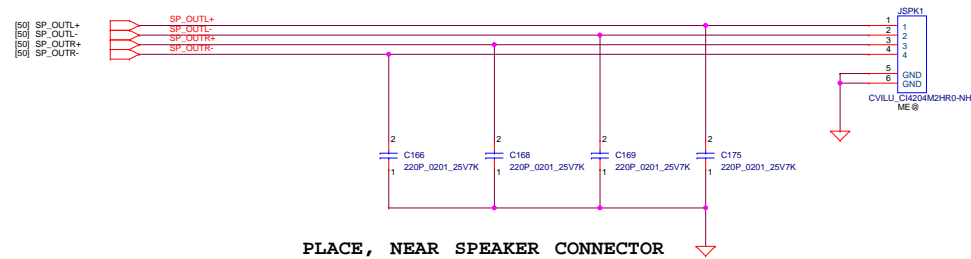
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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				Custom LA-C581P	0.5
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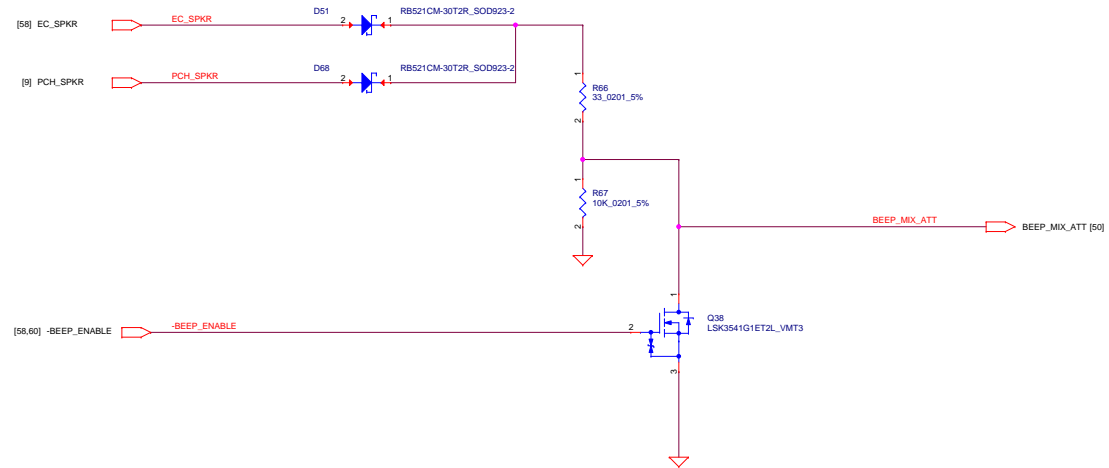
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Issued Date		Deciphered Date		Title	
2014/11/04		2016/12/31		AUDIO JACK SENSE	
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		Custom LA-C581P		0.5	
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Issued Date		Deciphered Date		Title	
2014/11/04		2016/12/31		AUDIO EXT MIC I/F	
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		Custom LA-C581P		0.5	
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				Custom	0.5
				Date: Thursday, August 13, 2015	Sheet 54 of 102



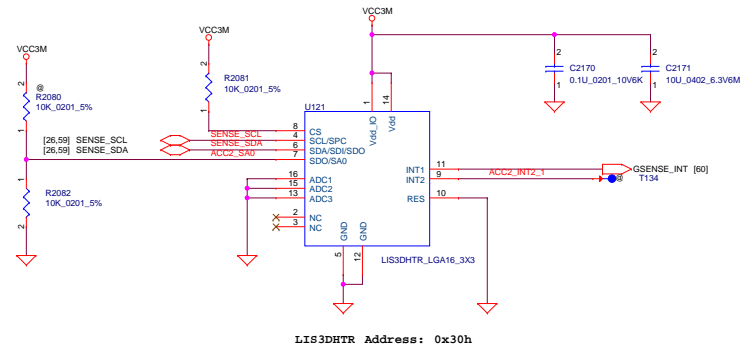
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title
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				Custom LA-C581P 0.5
				Date: Thursday, August 13, 2015 Sheet 55 of 102

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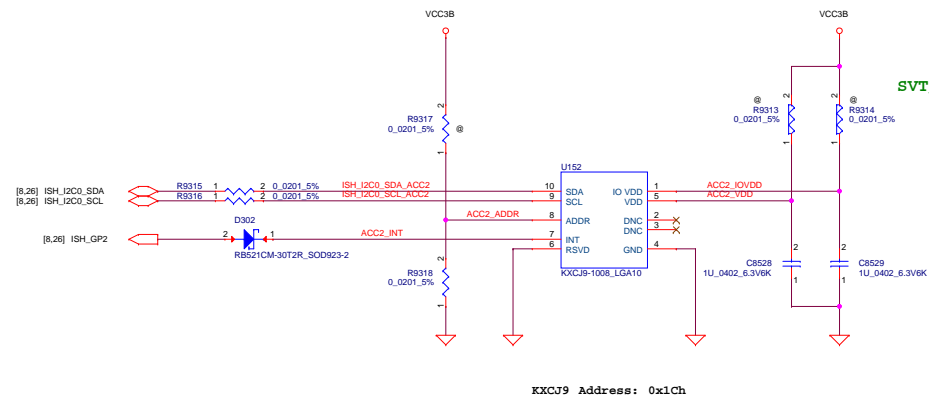
CS	Mode Selection
H	I2C Mode
L	SPI Mode

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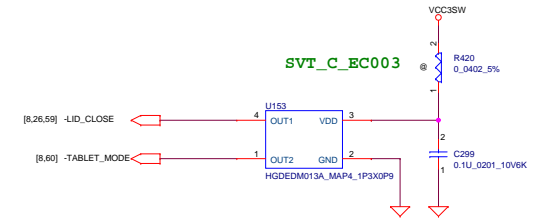
ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)



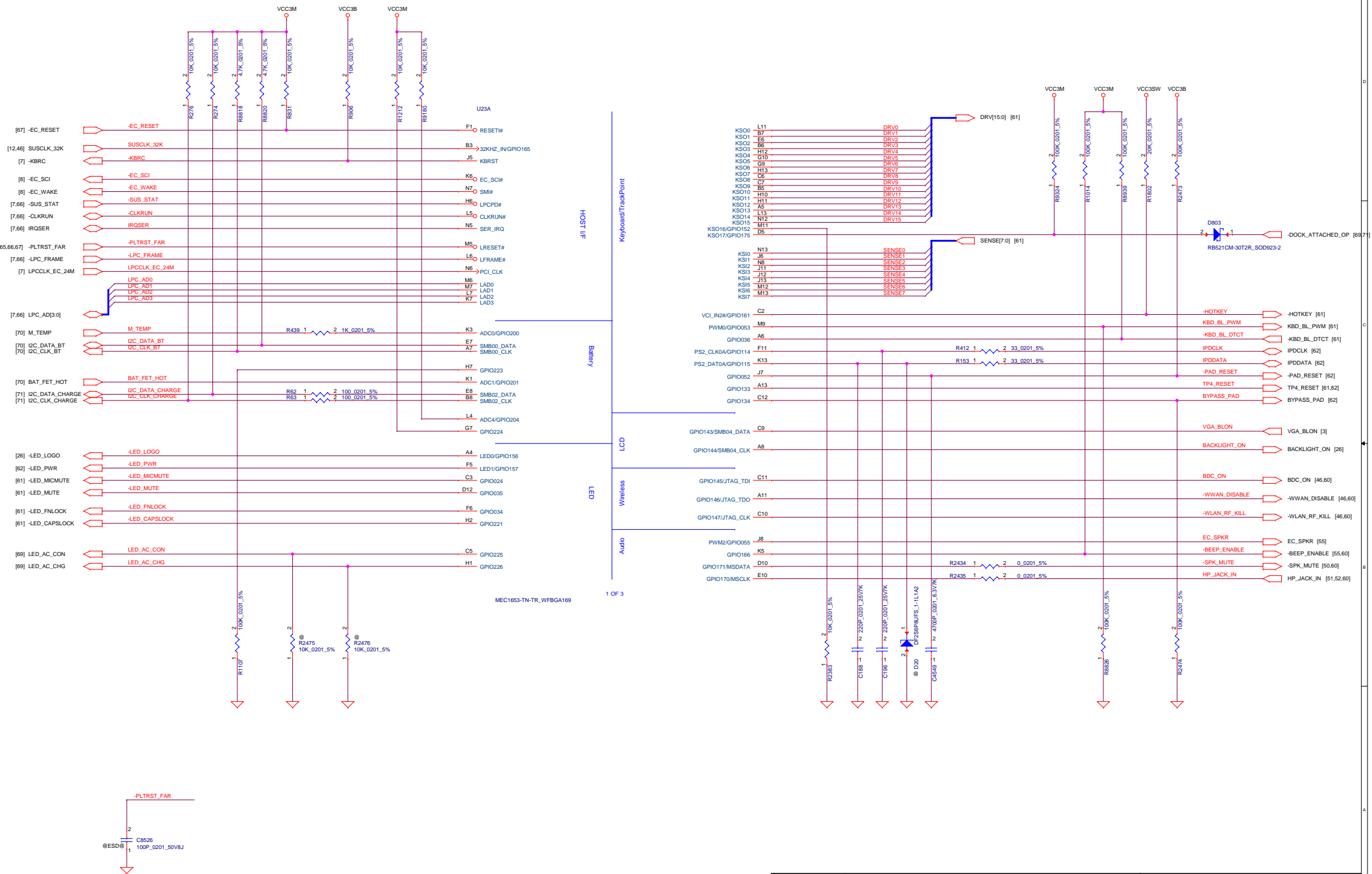
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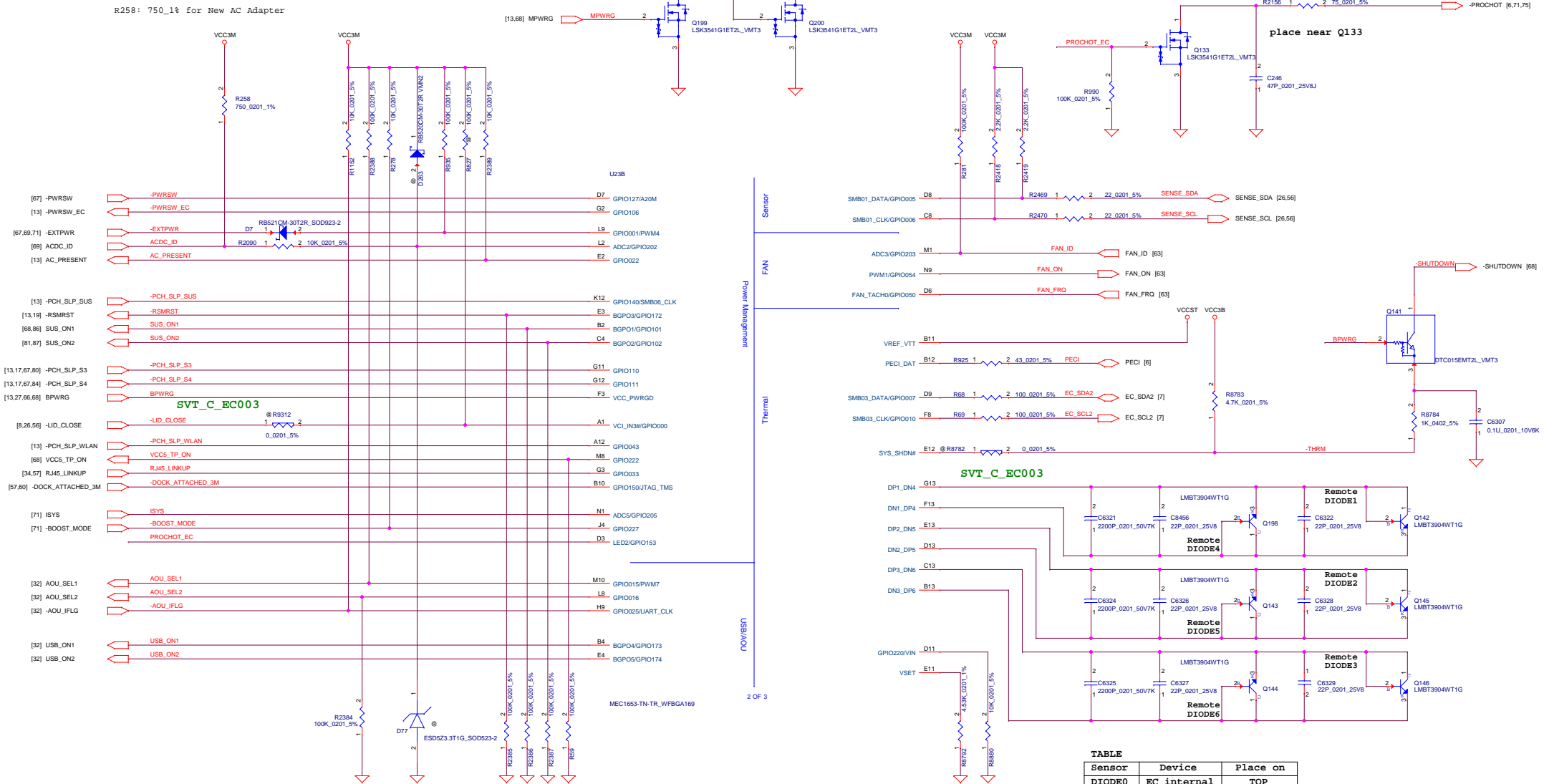
KXCJ9 Address: 0x1Ch



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			Custom	LA-C581P	0.5
			Date:	Thursday, August 13, 2015	Sheet 56 of 102

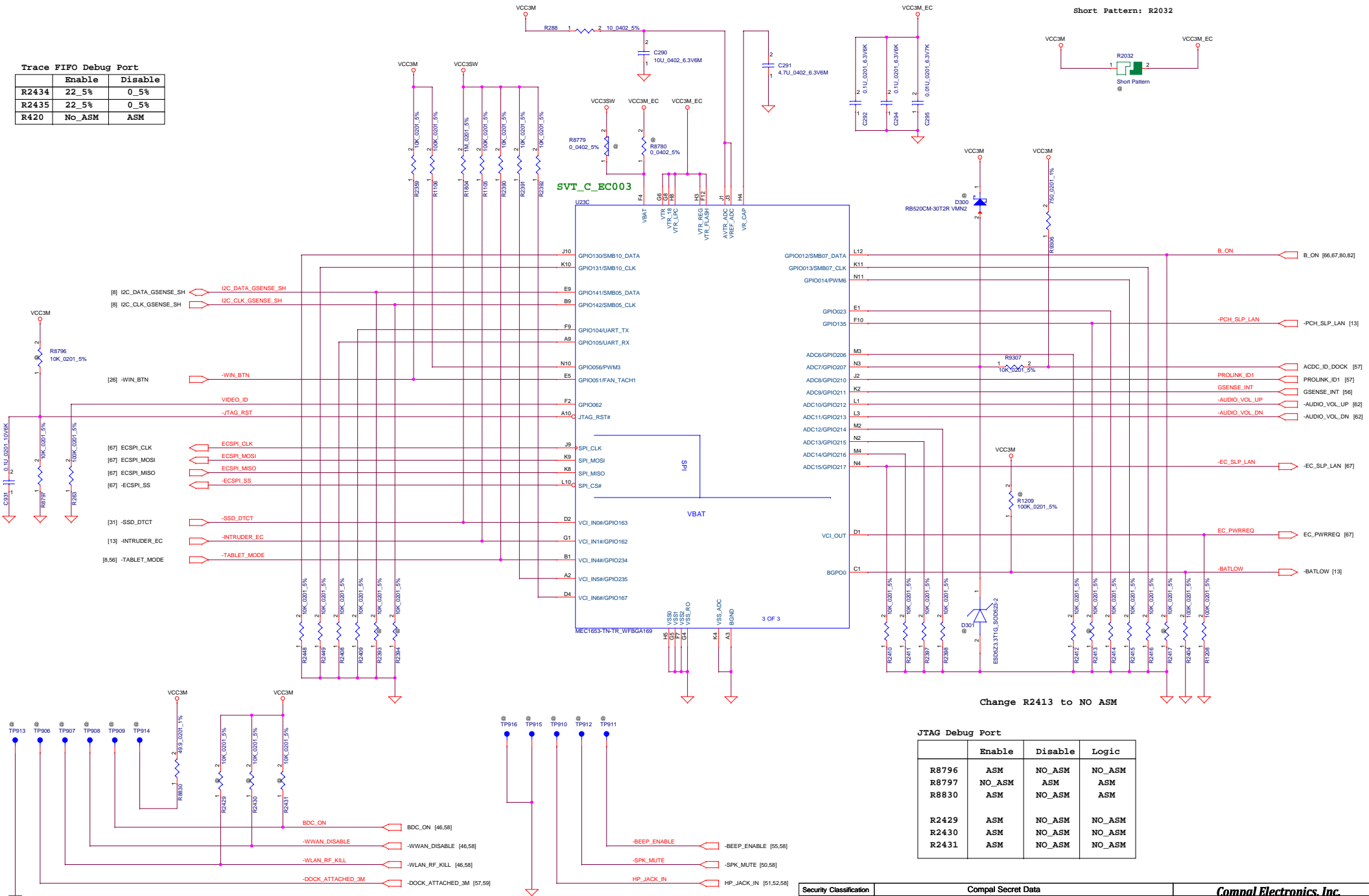


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				Date Thursday, August 13, 2015	Sheet 58 of 102



Trace FIFO Debug Port		
	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	No_ASM	ASM

SVT_C_EC005
Short Pattern: R2032

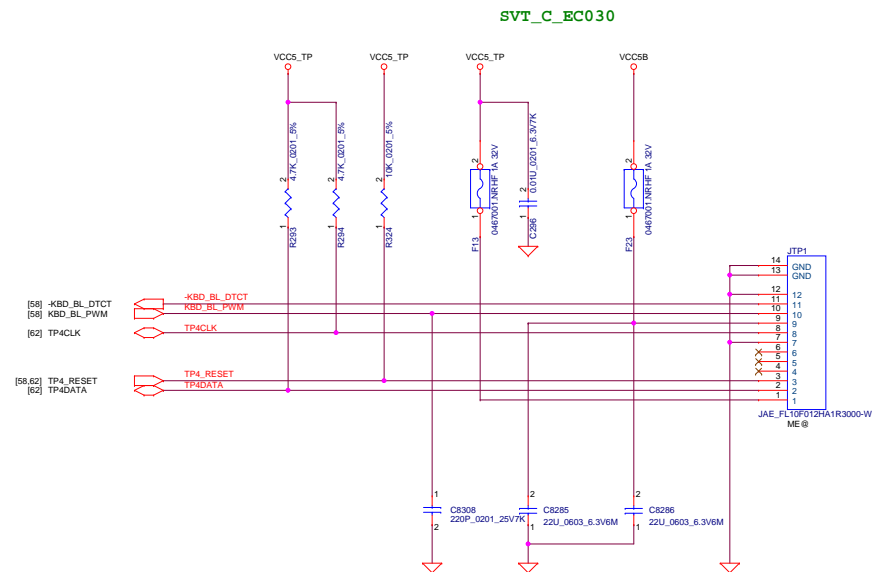
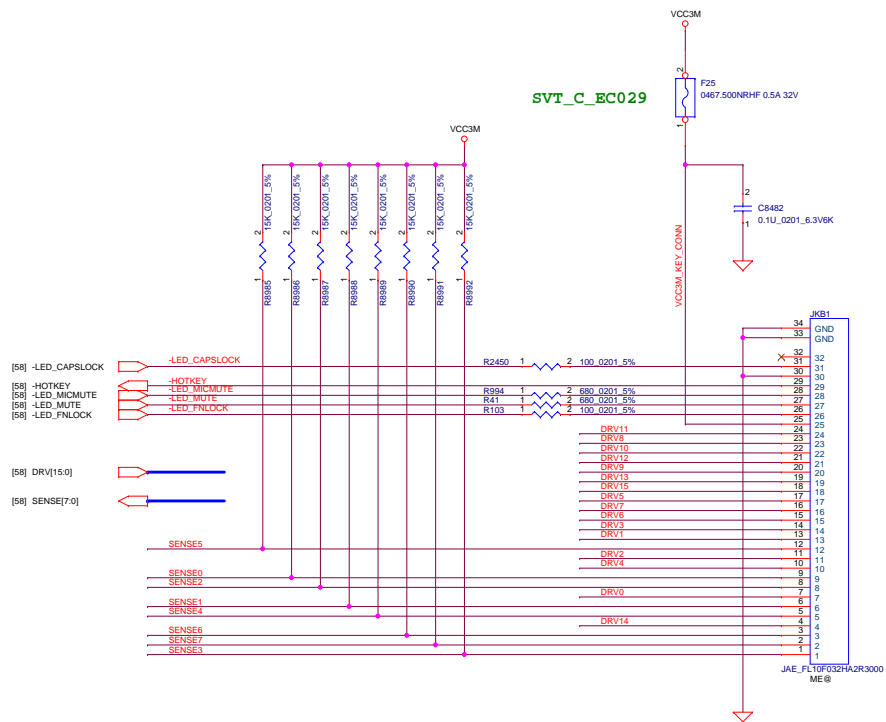


Change R2413 to NO_ASM

JTAG Debug Port

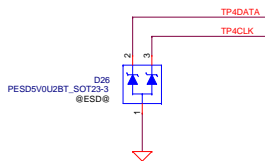
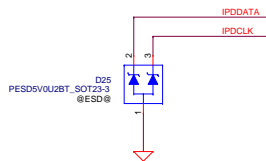
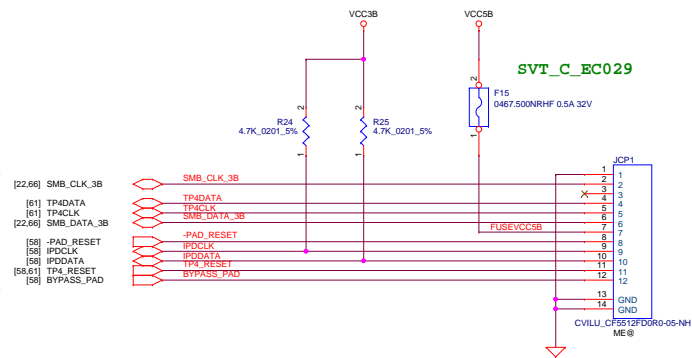
	Enable	Disable	Logic
R8796	ASM	NO_ASM	NO_ASM
R8797	NO_ASM	ASM	ASM
R8830	ASM	NO_ASM	ASM
R2429	ASM	NO_ASM	NO_ASM
R2430	ASM	NO_ASM	NO_ASM
R2431	ASM	NO_ASM	NO_ASM

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Issued Date		Deciphered Date		2016/12/31	
2014/11/04		2016/12/31		Compal Electronics, Inc.	
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Document Number		Rev		0.5	
LA-C581P		Date		Thursday, August 13, 2015	
Sheet		60 of 102			

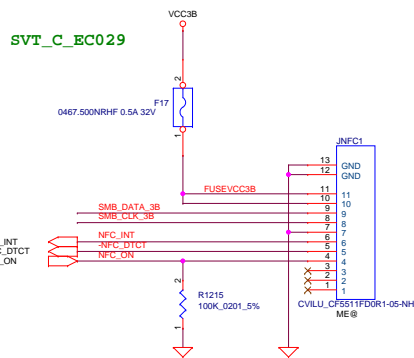


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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	KEYBOARD/TRACK POINT
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				Custom	0.5
				Date	Thursday, August 13, 2015
				Sheet	61 of 102

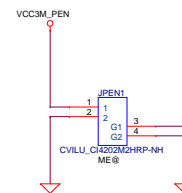
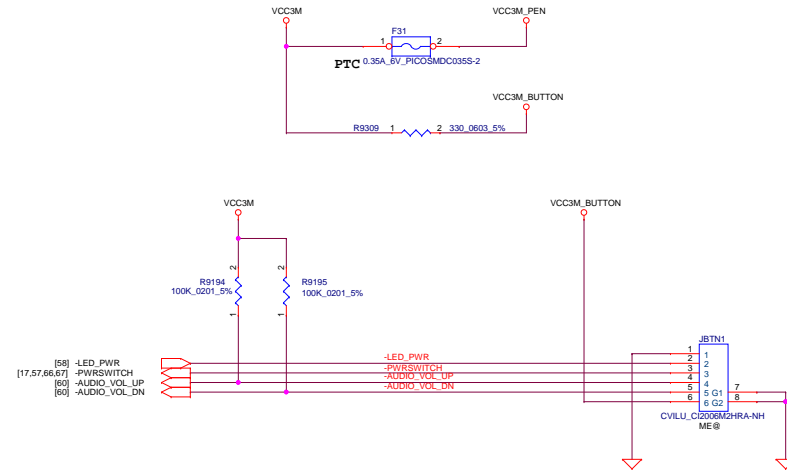
Clickpad



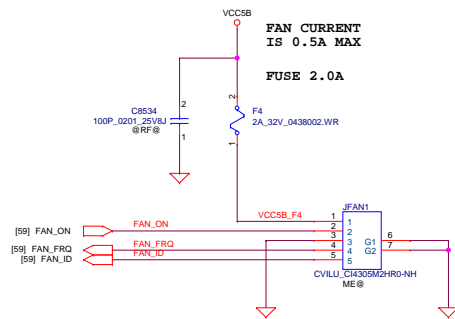
NFC



TO SUB BOARD



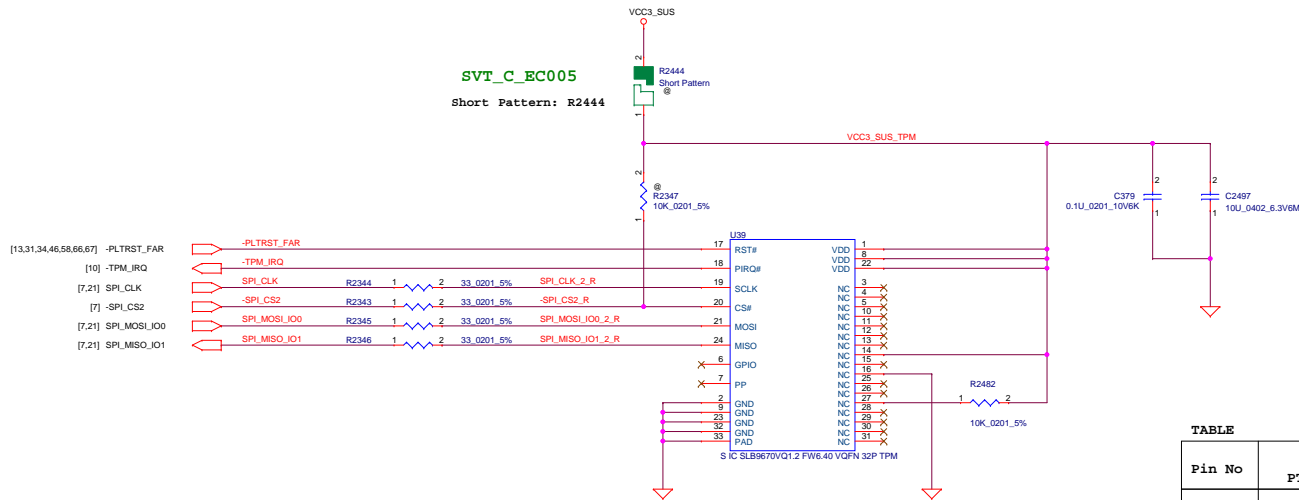
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				Document Number	0.5
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2014/11/04		2016/12/31		FAN CONNECTOR	
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		Custom		LA-C581P	
		Date		Thursday, August 13, 2015	
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-Change FW version of Infineon TPM to 6.40
-Change Nuvoton parts number to NPCT650LB0YX

TABLE

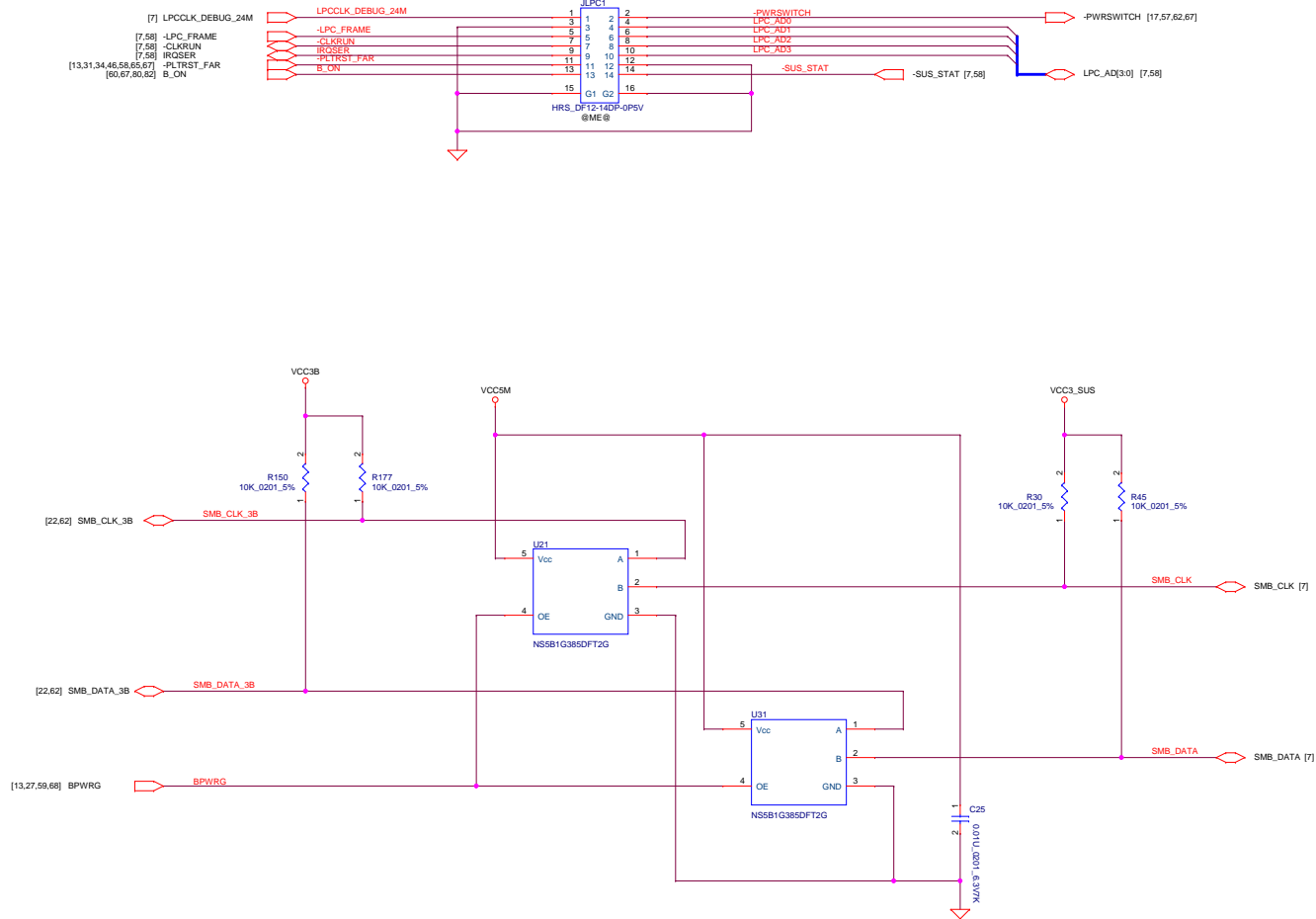
Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.40	Nuvoton NPCT650LB0YX
1	VDD	VDD	VSB
2	GND	GND	NC
3	GPIO	NC	GPX/GPIO2
4	GPIO	NC	PP
5	NC	NC	TEST
6	VNC/GPIO	GPIO	GPIO3
7	GPIO/VDD	PP	NC
8	VDD	VDD	VDD
9	GND	GND	GND
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	Reserved
13	VNC/GPIO	NC	GPIO4
14	VDD	NC	VDD
15	NC	NC	DNC
16	GND	NC	GND
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SCLK
20	SPI_CS#	CS#	SCS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VDD
23	GND	GND	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	(SERIRQ)
28	NC	NC	DNC
29	VNC/ GPIO	NC	GPIO0
30	VNC/ GPIO	NC	GPIO1
31	VNC	NC	NC
32	GND	GND	GND

TABLE			
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R220		ASM	NO_ASM

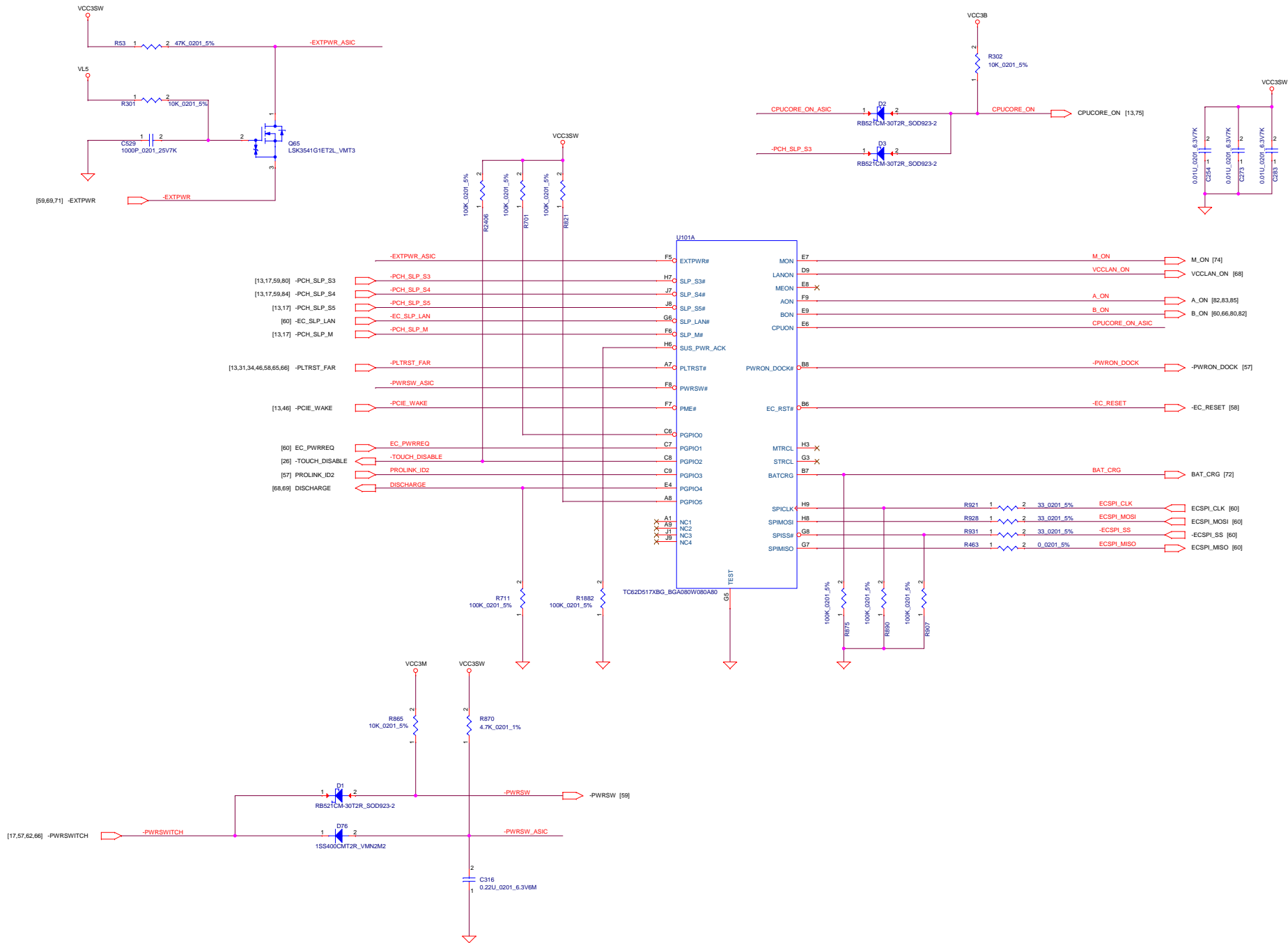
SVT_C_EC001

LOGIC

SVT_EC004

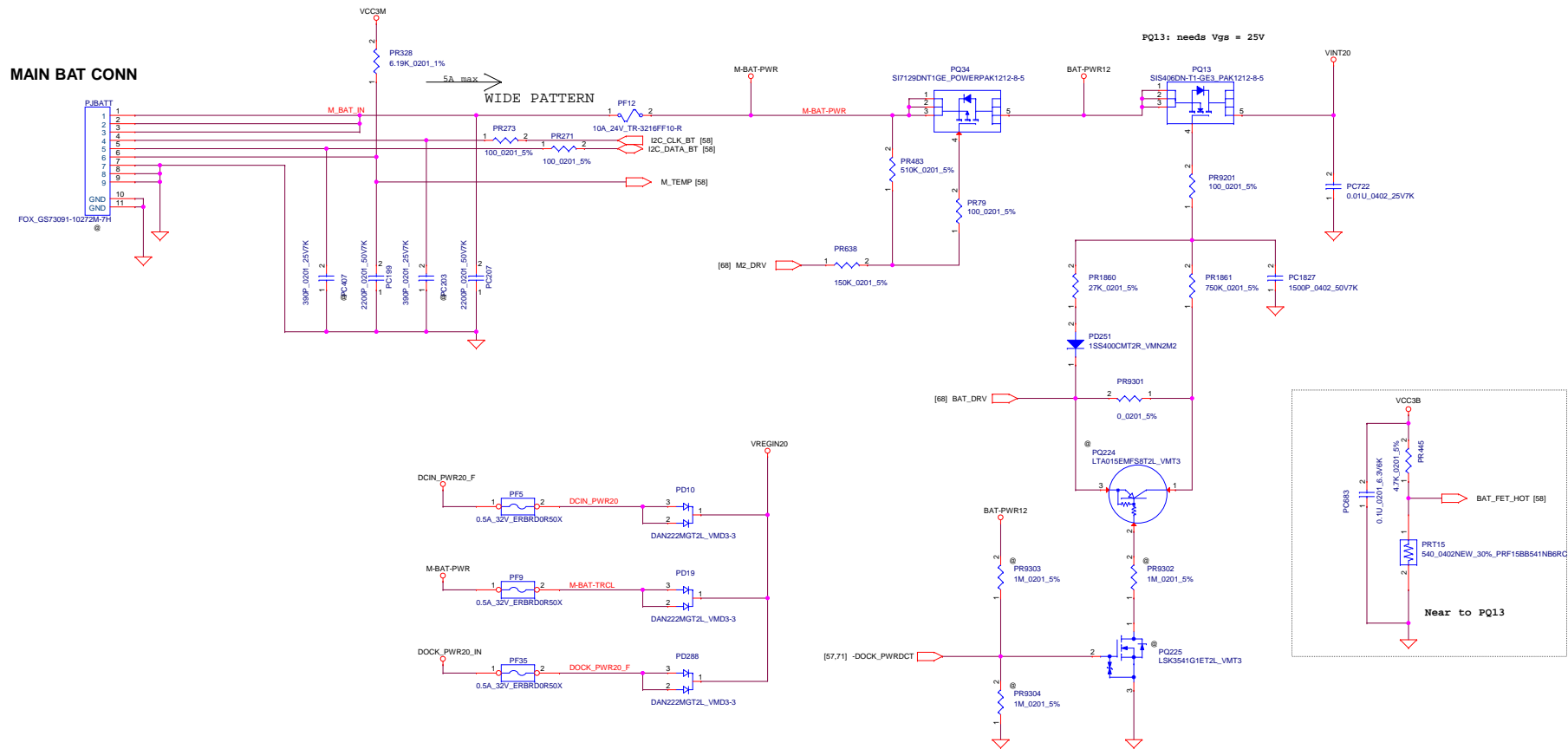


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				Date	Thursday, August 13, 2015
				Sheet	66 of 102
				Rev	0.5

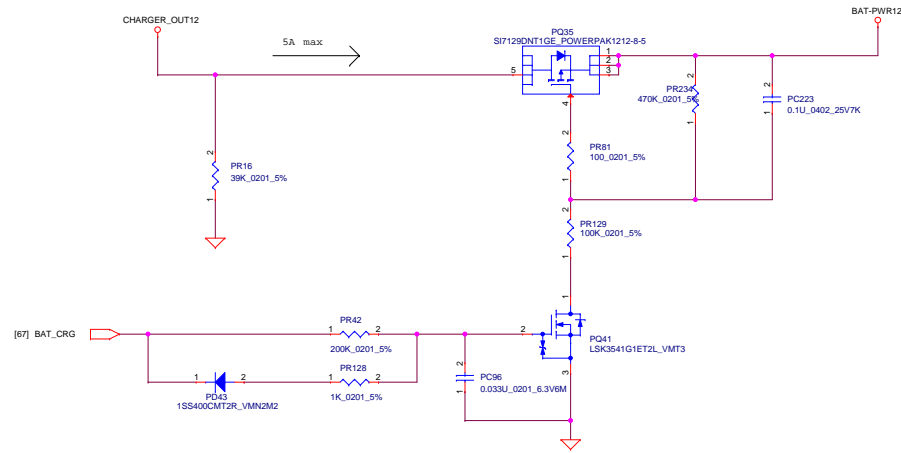


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		Custom		0.5	
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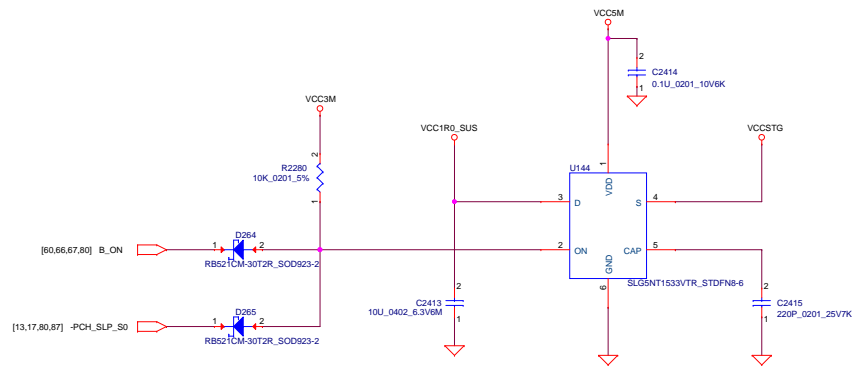
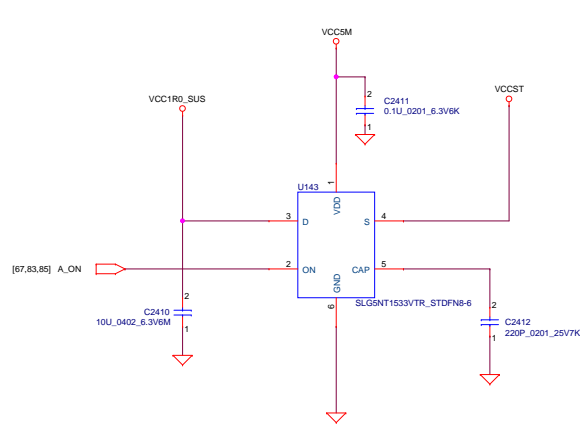
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R2205	12.4K	Ilim=40A	VCCGFXCORE
R2177	27.4K	Ilim=10A	VCCSA

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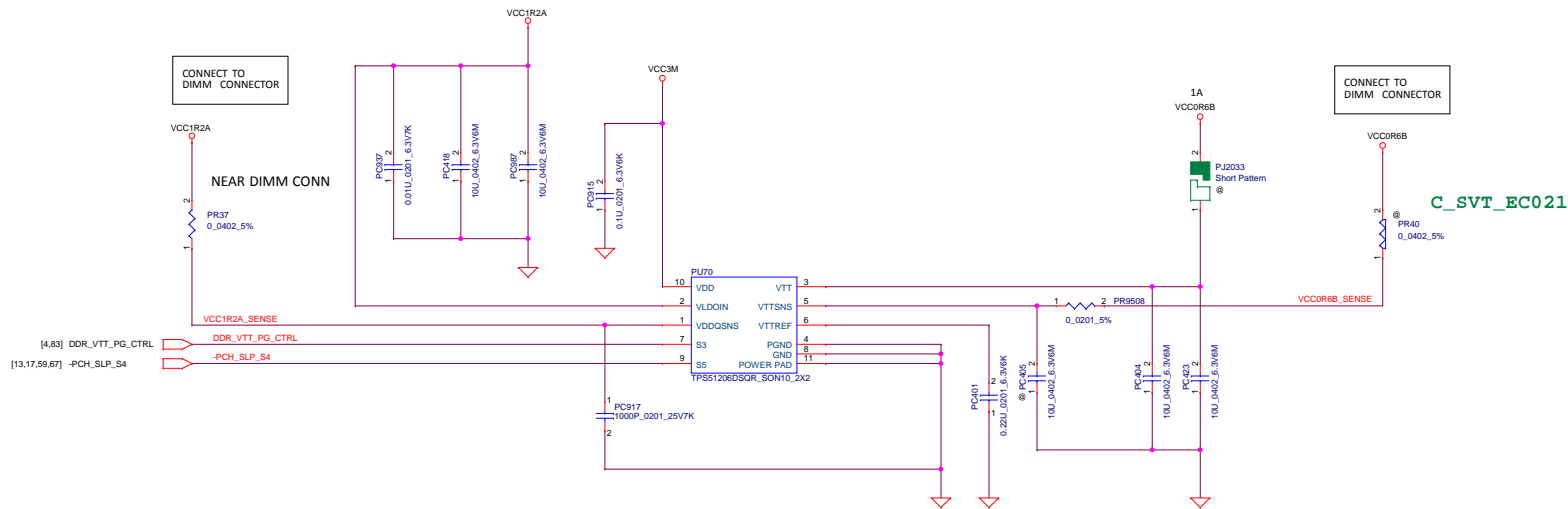
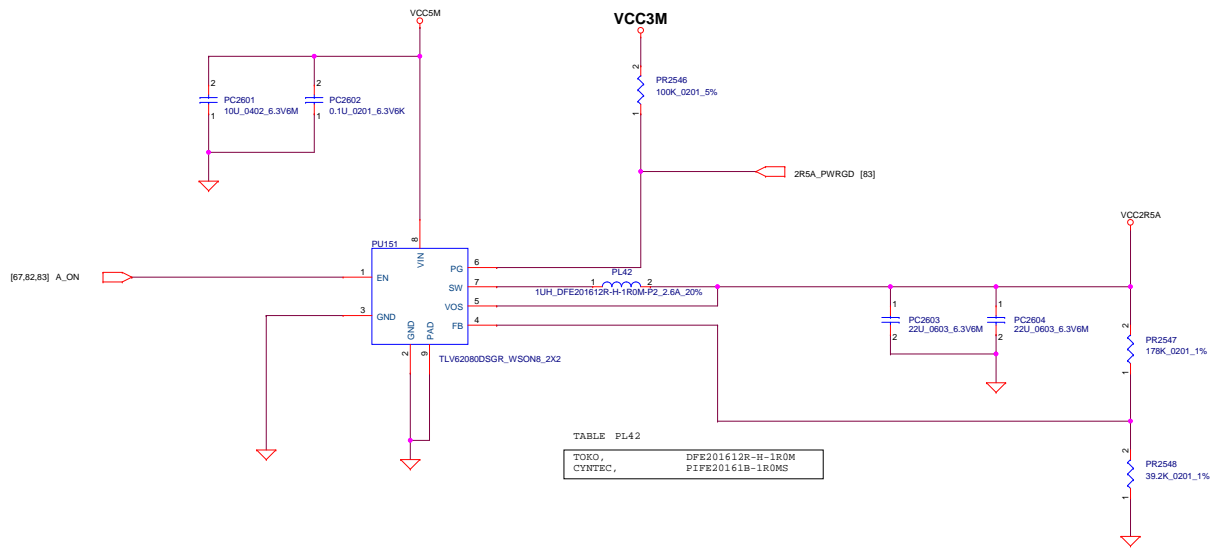
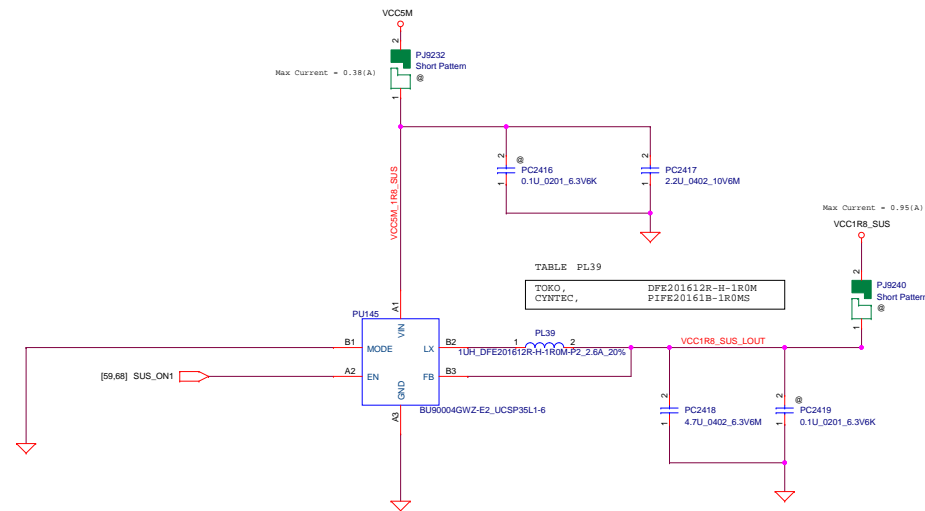


TABLE : TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)



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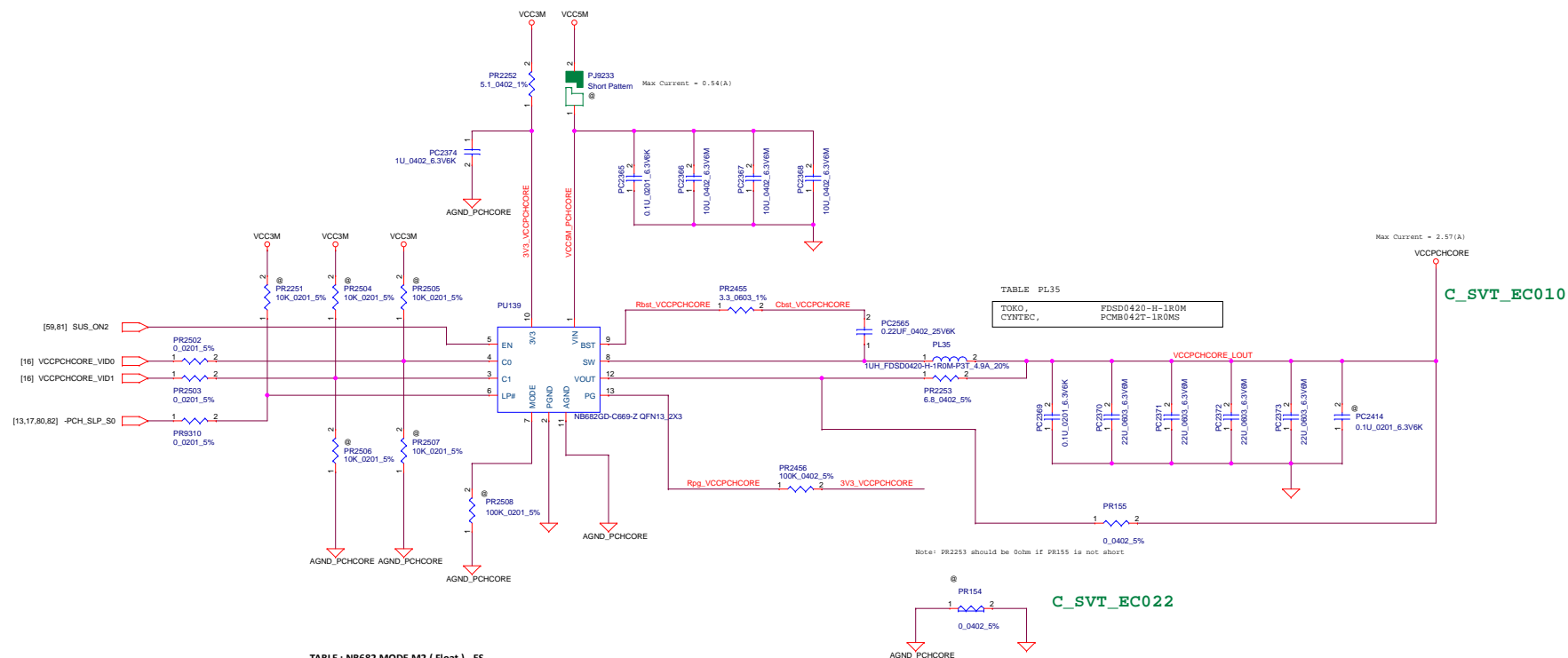


TABLE : NB682 MODE M2 (Float) - ES

LP#	C1	C0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V

← SLP_S0#

← DEFAULT

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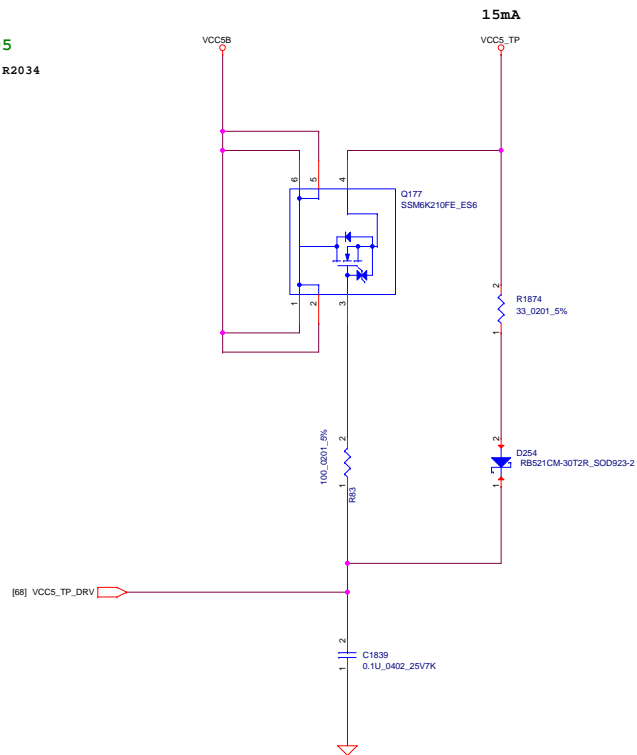
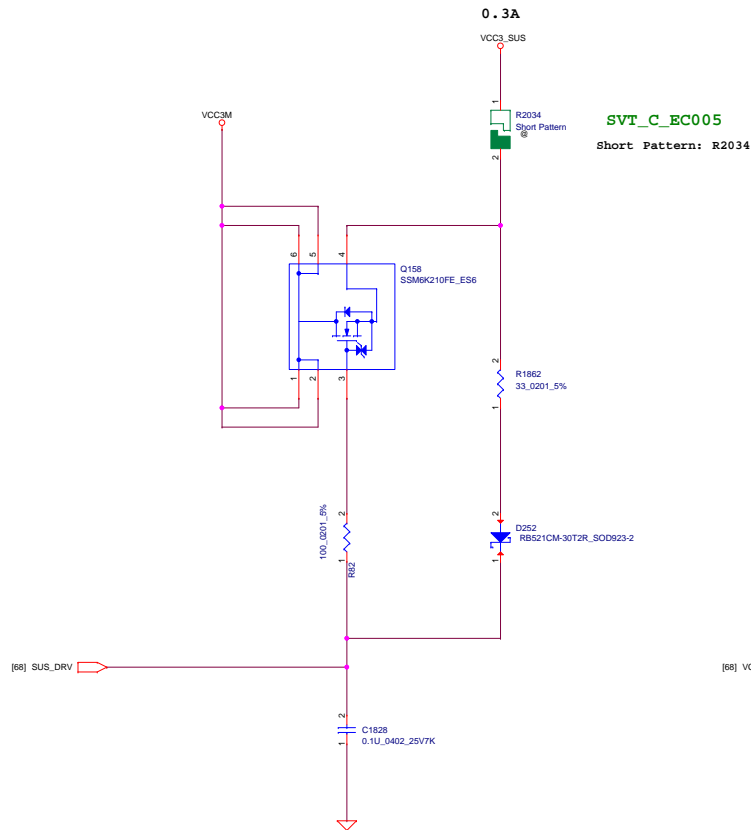
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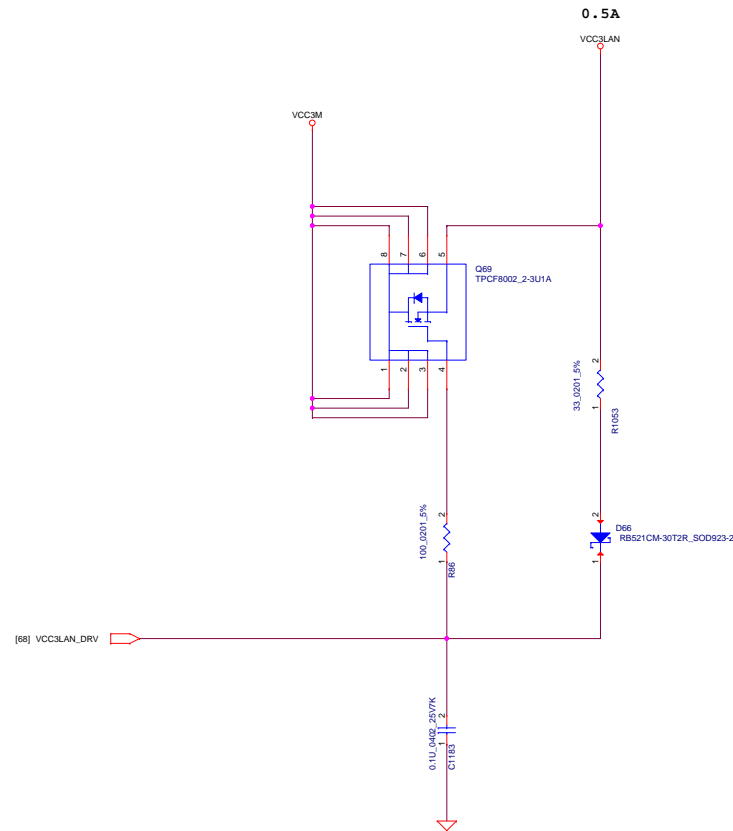
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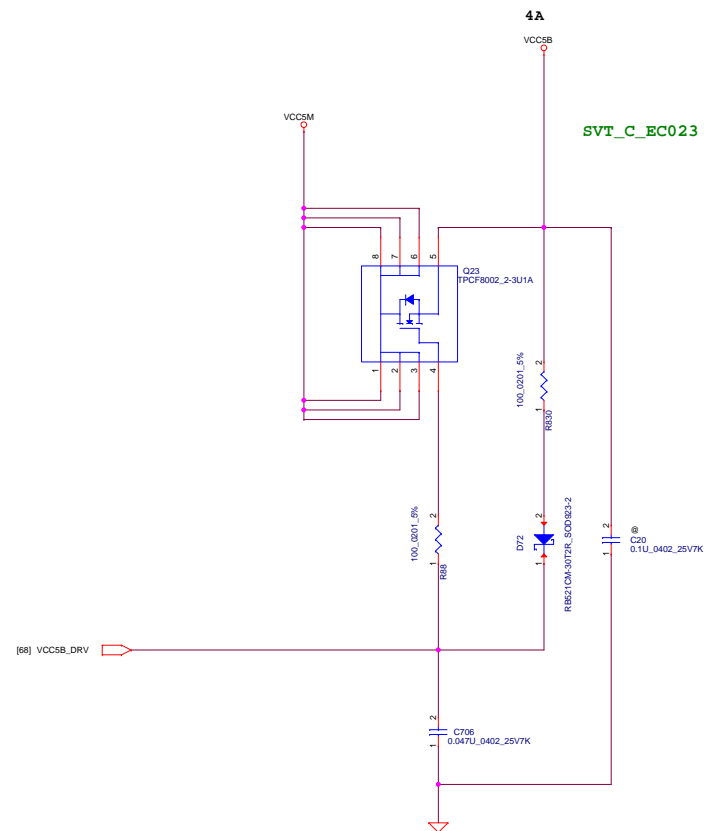
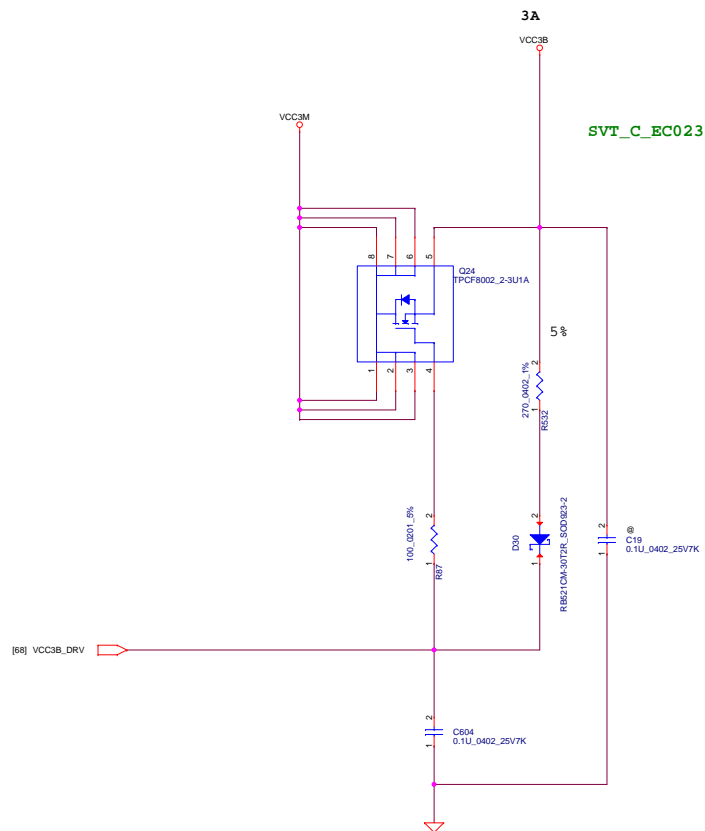
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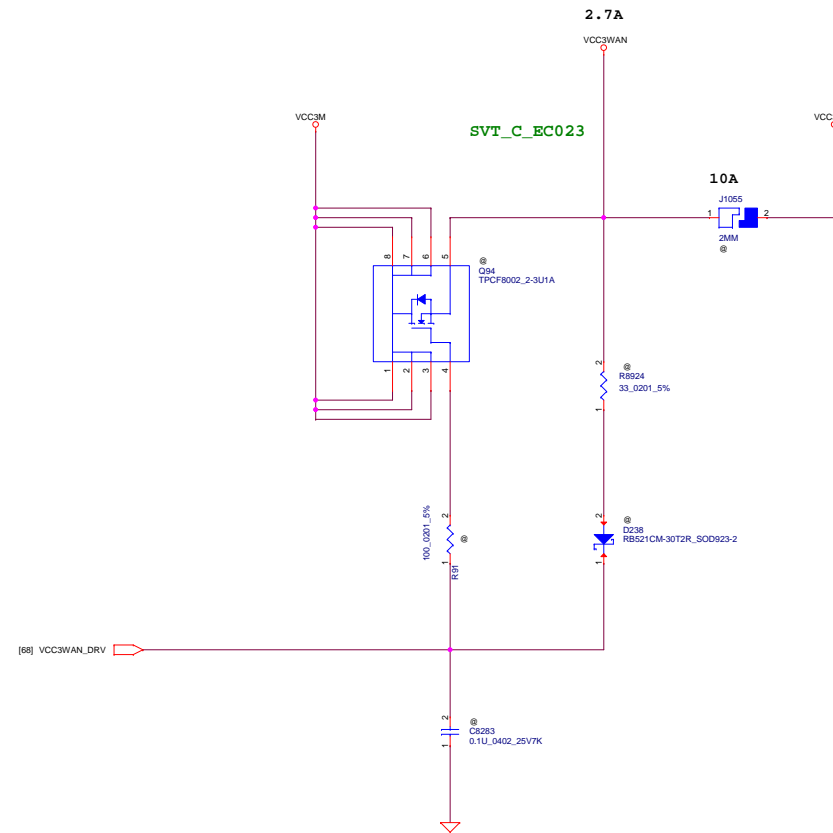
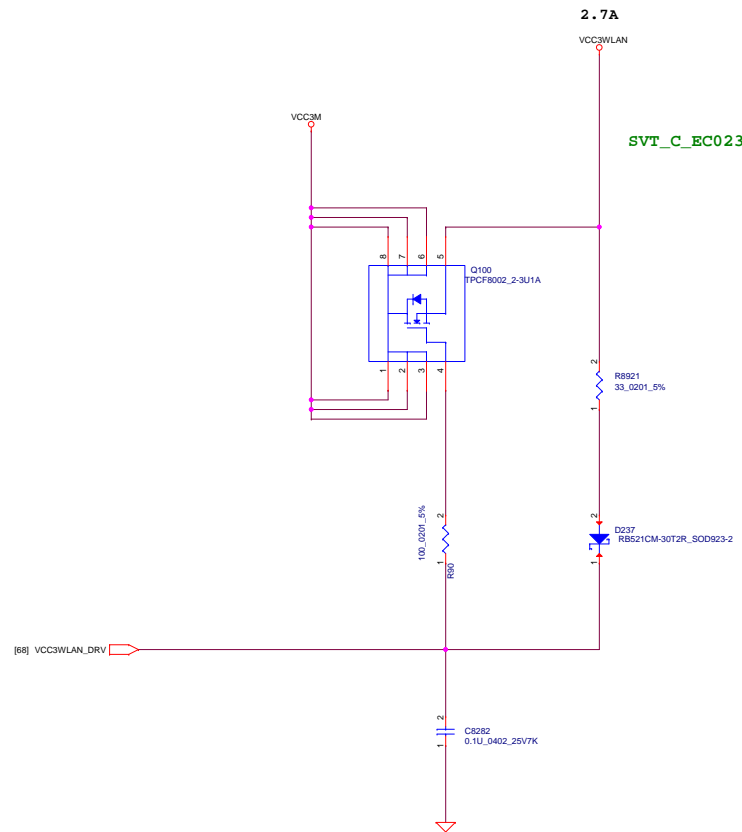
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TABLE

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R91	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

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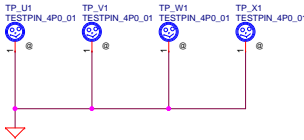
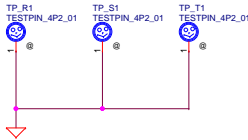
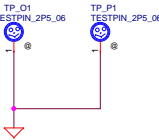
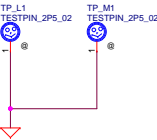
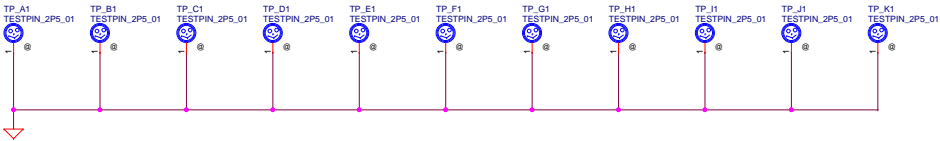
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Value	Hole Dia	Pad Dia		Qty
		TOP	BOTTOM	
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TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



NPTH



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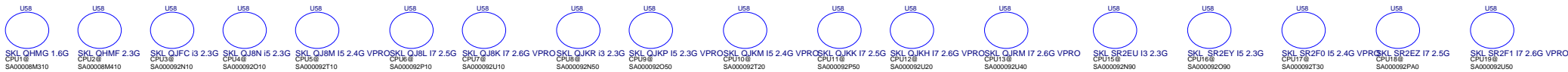
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SVT_C_EC025



SVT_C_EC028

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